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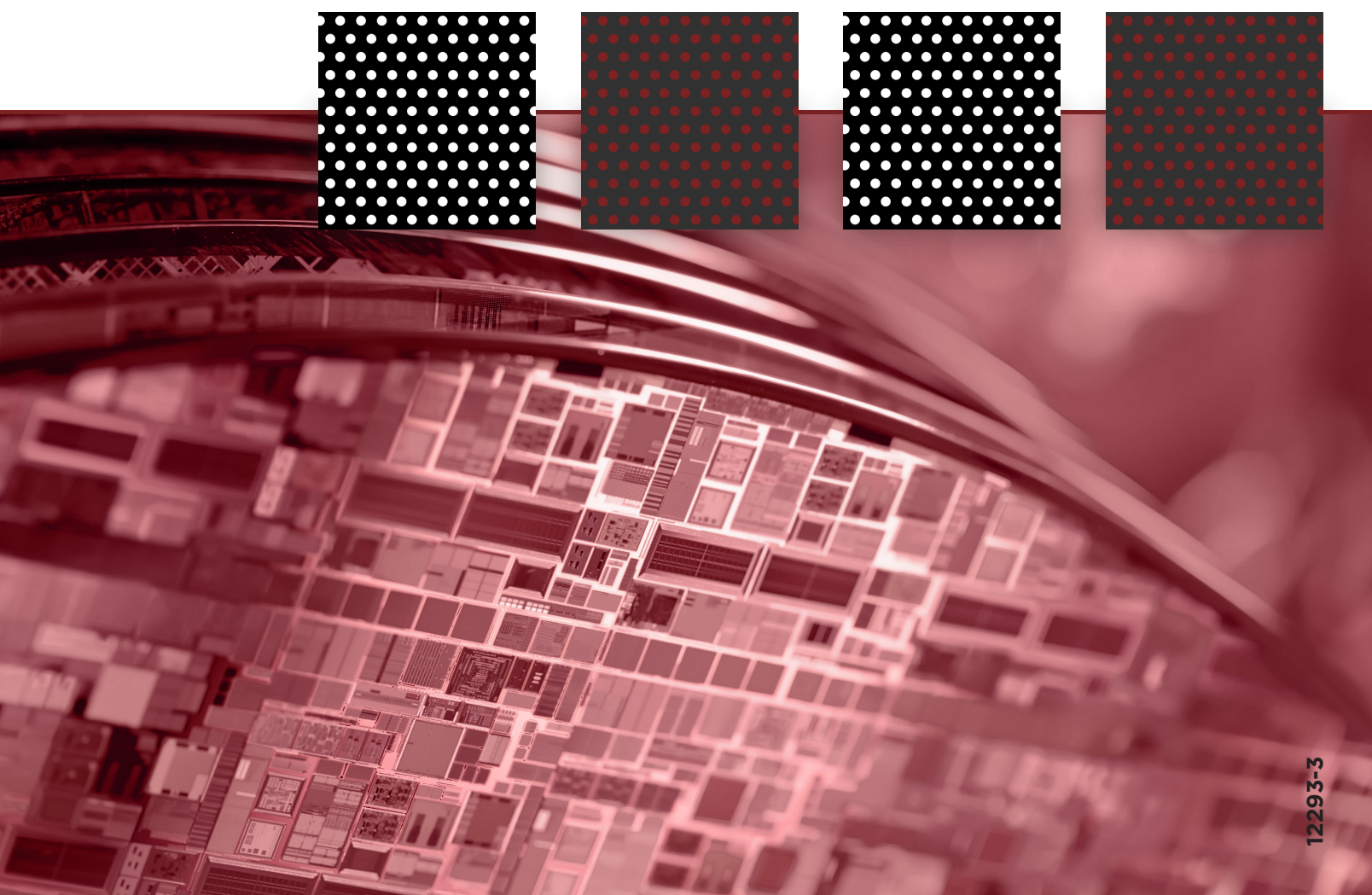
Media Size Discussions



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EDITORIAL

Media Size Discussions

Thomas Scherübl, *Carl Zeiss SMT GmbH*

During the recent Photomask and EUVL conference, there was a quite vivid and lively panel discussion. The topic was “What are the biggest challenges facing high NA EUVL in the areas of photomask and photoresist?" The program committees from Photomask and EUVL had put together high-level panelists representing the industry. After the initial statements and some discussion among the panelists, someone from the audience (I have to admit I do not recall the name anymore) brought up the question if the mask size for high-NA EUV should change.

The motivation is that high-NA EUV scanners will use anamorphotic masks which only cover half the field of the chip as compared to low-NA EUV scanners. For single-chip designs this leads, in combination with the black border, to stitching issues in imaging. The proposal, which was then very heavily discussed with the audience and the panelists, was to use 300mm technology to manufacture large 300mm “pizza” photomasks. Besides the benefit of solving the stitching problem, a large mask combined with a higher speed of the reticle stage of the scanner has the potential to increase the productivity of high-NA EUV scanners. Also, it was argued 300mm is a well-established technology in wafer manufacturing. Manufacturing tools exist that support the larger size. The step might not be so high to make the change even for a thin silicon substrate compared to existing (thick) low-expansion materials.

Having worked in the mask industry for almost 20 years, I remember at the beginning of my career that various photomask sizes based on glass substrates were common. The market expected that mask tools could handle all of them. However, over the years the 160mm square sizes have been established as the standard size for high-end mask technologies. As a consequence, almost all high-end mask-making tools support only this standard reticle. It is obvious that a change in media size will require large investments by the mask tool suppliers and industry. The questions of how this will be economically viable and how this can be financed are vital. The last major change in the semiconductor industry was the change from 200mm to 300mm wafers. Attempts to introduce 450mm failed for several reasons.

Will the mask size change for high-NA EUV? Currently, it is hard to predict. Besides the stitching, which might be solved also by alternative means, the productivity argument seems to be more compelling.

At the end of the panel, an industry veteran from the audience stood up and stated that he saw several discussions in his career to change the mask size but all failed due to cost reasons. Let’s see what the future will bring. Although ultimately the discussion was inconclusive, it was one of the greatest panels I have ever experienced. I wish to see more such vivid and open discussions in future editions of Photomask and EUVL.

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FEATURED ARTICLE **2022 BACUS BEST PAPER WINNER**

You Don't Need 1nm Contours for Curvilinear Shapes: Pixel-Based Computing is the Answer

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ABSTRACT

Enabled by multi-beam mask writing[1], curvilinear free-form ILT[2], and GPU acceleration[3], curvilinear masks are quickly becoming the norm in leading-edge masks, whether for 193i or for EUV, particularly for contact and via layers. An industry standard for compactly representing curvilinear shapes is being developed for SEMI through an industry working group. In it, Bezier, and B-spline "Multigon" formats are proposed to augment the piecewise linear polygons that are supported today[4]. Whether these infinite-resolution curvilinear formats are used, or piecewise linear polygons are used, there is a question of what constitutes a high enough vertex density to be of some pre-defined accuracy requirement. With these infinite-resolution curvilinear formats, the vertex density would be lower than with piecewise linear polygons for a particular accuracy requirement. But it is still useful to know what density is theoretically sufficient.

This paper explores the concept of rasterization and the mathematical dual between contours and pixel dose arrays given a particularly known resolution limit. The paper further argues that curvilinear ILT, practically speaking, is all computed in the pixel domain. And all curvilinear masks, with the notable exception of MWCO masks for 193i[5], are written with multi-beam machines using pixel dose arrays. The paper further argues that all images taken of the resulting masks, whether for inspection, disposition, or metrology are pictures taken as pixel dose arrays of some resolution with some image processing afterward.

Information theory is a branch of computer science that, among other things, gives insight into how much data is sufficient to represent any particular information content[6,7,8]. More generally, the field covers the idea of digitizing the analog world to some known limit of resolution. Rasterization is the digitalization of images that converts from contours, be it piecewise linear polygons, or some infinite resolution curves, to pixel doses of some pixel size and dose range. Contouring is the converse, going from pixel doses to geometric space. By understanding information theory, how curvilinear mask shapes are computed, and how curvilinear mask shapes are generated on the mask, we compute the theoretical limit of how much data is required to represent 193i and EUV curvilinear masks.

Introduction: Curvilinear Masks Representation Overview

There are various ways in which semiconductor masks can be represented. Having an efficient file format is essential to make sure that the mask-processing data path is not overloaded. This has encouraged the creation of different file formats like GDSII[9], Oasis[10], etc. to represent the mask data. Mask Data Preparation (MDP) is a very crucial step in mask making industry. The Multi-Beam Mask (MBM) writers have enabled curvilinear mask writing[13,14]. With the wafer process windows known to improve substantially with free-form curvilinear ILT[2], representing and computing with curvilinear shapes in MDP has gained in importance[12]. File sizes and computational complexity has become an increasing concern for the mask industry in the curvilinear era, prompting the industry to develop a SEMI standard[4].

The various file formats used for representing curvilinear masks can be broadly classified into 3 categories as depicted in Figure 1: Piecewise-linear format, Curvilinear format and Pixel-based format. Each of these categories has its own characteristics and can provide some benefits to represent the underlying mask data. Any of the representations can be made accurate within some pre-specified specification as required by the consumers of the data.

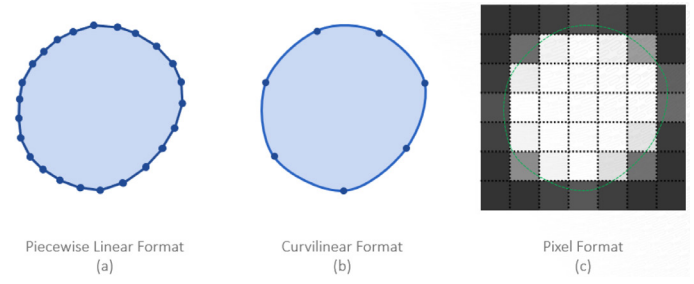


Figure 1. Classification of data representation formats for curvilinear shapes. (a) represents piecewise linear formats like GDS/OASIS, (b) represents curvilinear formats that may be based on Bezier / Splines and (c) represents pixel-based formats like Tiff or Bitmap file formats.

Piecewise-Linear Formats

The legacy piecewise-linear formats like GDSII or OASIS[9,10,11,12] have widespread adoption in the Electronic Design Automation (EDA) industry. Early file formats were mostly representing rectangular and Manhattan shapes. Since the mask data was mainly arrays or repetitions of simple shapes, hierarchical representation avoids unnecessary repetition of the same data in formats like GDSII. As the technology nodes advanced, the need for Optical Proximity Correction (OPC) made each instance of the mask shapes different based on the lithographic context around that instance, reducing substantially the ability to deploy hierarchy to compress data. Repeated

chips on a reticle may be represented by hierarchy for 193i chips, but complex effects of EUV threaten to require different OPC/ILT for each chip along the Y axis, too. OPC also gave rise to an increase in the number of vertices required to represent the data as shown in Figure 2. This in turn created the need for data compression. Formats like the OASIS format took information-based data compression a little further by using fewer bits to represent only differences in between adjacent coordinates, and by storing X or Y coordinates in alternating Manhattan coordinate sequences as first introduced for the DEF format[15].

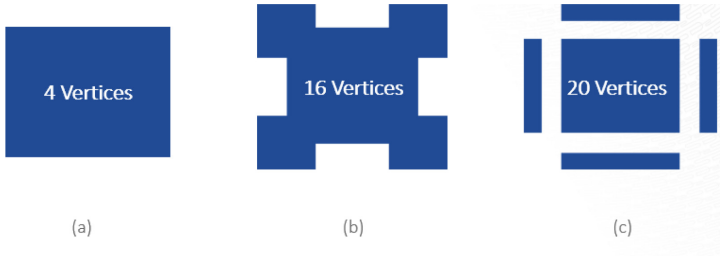


Figure 2. Increase in vertex count with OPC. (a) represents a simple mask shape that gets converted to (b) or (c) with OPC.

With MBM writers, curvilinear masks can be written at the same time with the same precision as Manhattan masks. Since wafer quality is better with curvilinear masks output by curvilinear ILT, curvilinear masks are projected to become common among leading-edge masks for both 193i and for EUV.[16] Curvilinear shapes are represented as piecewise-linear polygons causing a data explosion as shown in Figure 3.

To understand the implication of piecewise linear formats, we can just try to figure out the file size for different circle array patterns as described in figure 4. A circle array, arranged in this way, represents a good upper bound on the packing density of vertices required to express any manufacturable set of curved shapes on any mask. With this case, we can analytically estimate the number of vertices per circle and the number of circles per μm^2 of mask area. Since we cannot guarantee that every shape in an ILT mask for the EUV process will be identical, we must assume a representation of flat (no hierarchy) data. We can still consider representation with deltas as defined in OASIS file format. So, say each vertex takes 2 bytes of memory to save on disk. The estimated file size for some example test cases is shown in table 1 for a full reticle (104mm x 132mm) design.

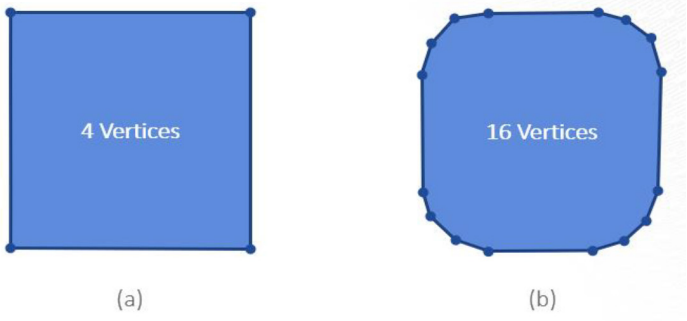


Figure 3. Example showing an increase in vertex count for curvilinear designs. (a) simple Manhattan data. (b) Piecewise linear representation of curvilinear data.

The circle array in figure 4 is placed such that 3 nearby circles form an equilateral triangle with a side equal to the pitch of the design. Such a triangle covers 1/6th of the area of each circle that it goes through. We can also say that each such triangle covers 3 x 1 / 6^{th} = 1/2 the perimeter of the entire circle and thus half the vertices.

The number of vertices in a circle can be calculated using the following equation:

$$\textit{Number of vertices per circle} = \frac{\textit{Perimeter}}{\textit{Segment Length}} = \pi \times \frac{\textit{Diameter}}{\textit{Segment Length}}$$

Since each equilateral triangles cover half a circle, the number of circles per μm^2 can be computed using the following equation:

$$\textit{Number of circles per } \mu m^2 = \frac{1}{2} \times \frac{1000nm \times 1000nm}{\textit{Area of equilateral triangle}} = \frac{1}{2} \times \frac{1000nm \times 1000nm}{\frac{\sqrt{3}}{4} \times Pitch\_nm^2}$$

Using equations (1) and (2) and considering 2 bytes per vertex for some file size estimations, we computed table 1 on the following page.

Based on the information from table 1, a reasonable upper bound on a EUV mask with curvilinear geometries can take greater than 100 Terabytes of data to represent a full reticle design with no hierarchy. This is certainly too expensive for the data path in MDP.

Curvilinear Formats

In order to assuage the effects of curvilinear design on file size, the mask industry is currently working on a Bezier-based curve format to be adopted as a SEMI standard[4] that is suitable to represent curvilinear shapes. An example of such formats is shown in Figure 5(b).

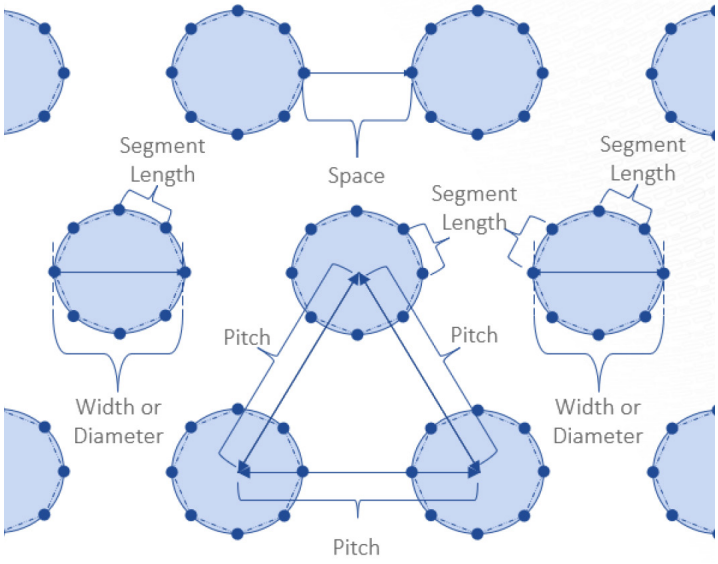


Figure 4. A circle array pattern representing a curvilinear design with parameter definitions for Diameter, Space, Pitch and Segment Length.

Bezier curve is a parametric curve that utilizes control points to define a smooth curve. The curve format will have some control points on the curve and some additional control points that may be either implicit (i.e., based on curve control points and some pre-defined parameters) or explicit. The implicit Bezier-based curvilinear format has huge potential to reduce the effective vertex count required to represent the shapes. In the curvilinear format's case, the vertex counts just represent the number of explicit control points required to faithfully represent a curvilinear shape. Interpreting the data from table 1 and assuming that we can use an implicit Bezier-based curvilinear format, it can be estimated that such a format will have effective vertex density (or control point density) in the order of the data corresponding to 10nm or 20nm segment length. Thus, file sizes may be limited to an average case of 10TB - 30TB which is about a 10x reduction compared to piecewise linear formats.

Circle Diameter (nm)	Pitch (nm)	Segment Length (nm)	Vertex Density (Count per μm²)	Full Reticle File Size (TB)
100	150	1	~16000	~440
100	150	5	~3200	~88
100	150	10	~1600	~44
100	150	20	~800	~22
100	200	1	~9000	~250
100	200	5	~1800	~50
100	200	10	~900	~25
100	200	20	~450	~12.5
150	225	1	~11000	~300
150	225	5	~2200	~60
150	225	10	~1100	~30
150	225	20	~550	~15
150	300	1	~6000	~160
150	300	5	~1200	~32
150	300	10	~600	~16
150	300	20	~300	~8

Table 1. File size estimations for the circle array are shown in Figure 4 with different parameters.

Pixel Format

Semiconductor masks can also be represented using pixels. Each pixel value in such a case would just represent the percentage area of the pixel covered by the shape that the pixel needs to represent. Figure 1(c) represents such an example of pixel-based representation. There are many formats like TIFF or BITMAP format that can be used to represent pixels. In general, pixel-based representation of mask data is used for eBeam or ILT simulations. Although it represents the natural language of Multibeam Mask Writers, it is too expensive in terms of file size.

There are approximately (104mm x 132mm / (16nm)2) ≈ 50x1012 pixels in an entire reticle if we consider a pixel size of 16nm. If we use 2 bytes to represent each pixel, then a pixel-based format without any compression may take 100TB of file size. The good thing about pixel format is that this is a constant number irrespective of design complexity. This suggests that if the eventual target is to write masks using MBM writers, it may be more useful to use a pixel-based format instead of piecewise linear formats. An alternative to pixel format would be a format that is pixel-based-computing-aware and uses it to represent the data using piecewise curvilinear format thus getting a greater reduction in file size to a value less than 10TB.

Fundamentals of Pixel-Based Computing

Pixel-based computing is the basis of many simulation software and graphical tools. It has been used in Computer-Aided Design (CAD) tools for various physical simulations. The most advanced semiconductor masks written today already use pixel-based computing, accelerated by GPUs.

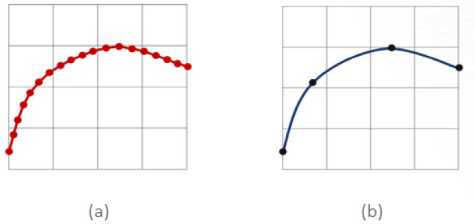


Figure 5. Section of a curvilinear shape. (a) Piecewise-Linear Format (b) Bezier/Spline-Based Curve Format.

Rasterization

The MBM writers get the input design in some geometry format. In order the write the mask, the writer needs to know the amount of dose it needs to project at a certain location on a mask. To compute the dose amount, the machine internally runs a process called rasterization. Rasterization is a process that converts the geometrically-expressed shapes into a pixel map based on the area of the pixel covered by the shape as shown in Figure 7.

Pixel Domain Sampling

Rasterization can also be defined as the digital sampling of vector shapes. Pixel domain sampling has roots in digital signal processing. Just like audio signals are sampling data in 1-D, rasterization is sampling data into a 2-D map of pixels. So, it must follow the Nyquist Rate to capture all relevant information. It also adheres to the information theory, which among other things says that the minimum volume of data required to represent something, is indeed, limited

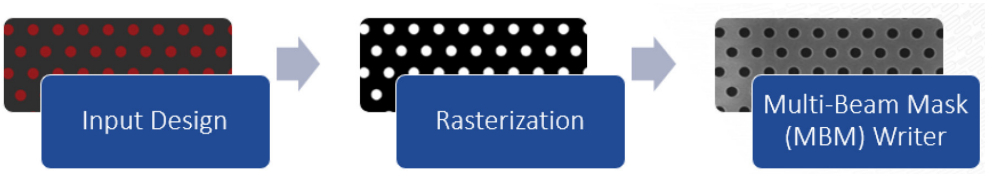


Figure 6. Processing Steps in Multi-Beam Mask Writers.

Figure 7. Rasterization of an input contour into a pixel grid based on area coverage.

by the amount of information, contained in that data.

We can say contour geometry and pixels are duals, and whatever you can do in one domain can also be done in the other. The duality holds true only if we follow the resolution limit that is determined by the Nyquist-Shannon Sampling Theorem. It seems that the curvy geometries require a lot of data to be represented faithfully. However, the information content is limited. If, at some point in the entire MDP flow, we are going to represent the same data in the pixel domain, then, we have an implied limit on the information content. This limit is going to be a function of the number of pixels or the pixel size.

We can get some intuition of how the Nyquist rate affects the pixel sampling using some examples with different grid alignments. In the pixel domain, the Nyquist Rate limits the pitch, which in line:space patterns is the line+space. Figure 8 assumes an equal L:S pattern. An important intuition about rasterization is that a given pattern must be discernable irrespective of the pixel-grid alignment. The example in figure 8(a) is a case of perfect grid alignment. It is easy to determine the original design from pixel values as a clear boundary can be seen in the pixel data between pixels with a value of 0.0 and those with a value of 1.0. So, this is not an ambiguous example. The example in figure 8(b)

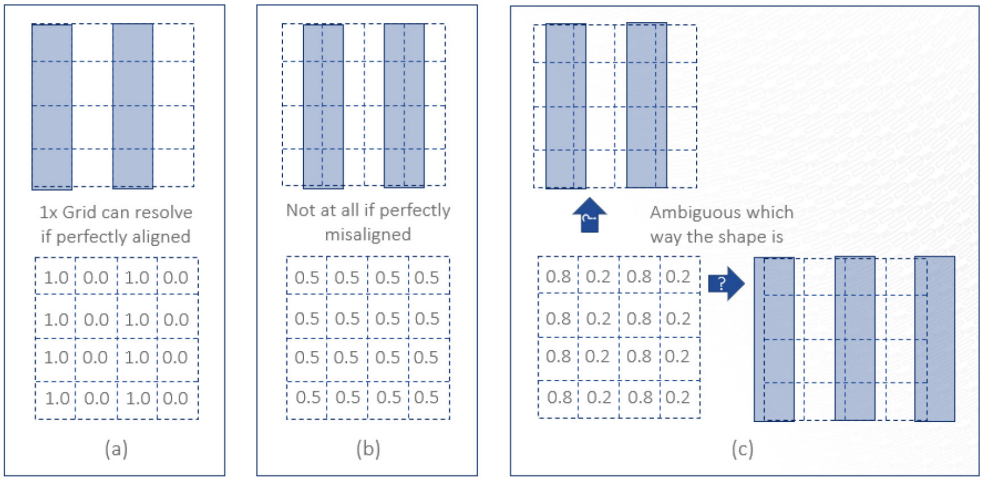


Figure 8. Rasterization of simple line-space pattern with line width and space equal to pixel size across different pixel alignments. (a) Rasterization grid is aligned perfectly with the input line. (b) Rasterization grid is 50% aligned with the input line. (c) Rasterization grid is 80% or 20% aligned with the input line.

shows 50% misalignment or perfect misalignment, where all the pixel values are 0.5. From the pixel data, we cannot restore the L:S pattern because that information has been lost in the translation to the pixel domain. The last example from figure 8(c) shows an 80%/20% split in alignment. This case is again ambiguous as there are 2 possibilities of line-space patterns rasterizing to the corresponding pixel values. Note that the Nyquist rate says the sampling rate for the pitch needs to be "greater than 2x" and not "greater than or equal to 2x" for such reasons. So, the Nyquist criteria also govern the mask rules in the pixel domain.

Pixel Dose Equivalence

The exact vertex location is never used for wafer quality evaluation, and it is not relevant for mask writing or inspection as you never see sharp corners. So, there is no so-called accurate polygon in the pixel domain. In fact, both red, as well as blue curves from figure 9, rasterize to the same pixel values. Hence, rasterizations inherently act like low-pass filters. As far as we are in the pixel domain, red and blue contours have the same information content due to pixel dose equivalence. Here, the red contour uses much more data (in terms of vertices) in conveying the same information (in terms of pixels). Therefore, the upper bound on the maximum number of vertices required is governed by pixel size using the following equation:

A shape like the red contour is not

$$\text{Number of effective vertices} \approx \left(\frac{\text{contour perimeter}}{\text{pixel size}}\right)$$

repeatably and reliably manufacturable. So real shapes on production masks are likely to require fewer vertices.

Pixel-Based Computing for Curvilinear Masks

Pixel-Based Mask Writing

Most advanced masks are written by MBM writers and are therefore written using pixels. We are limited by what multibeam can write. Mask writer's pixel size governs the smallest printable feature size. Figure 10 shows 3 examples

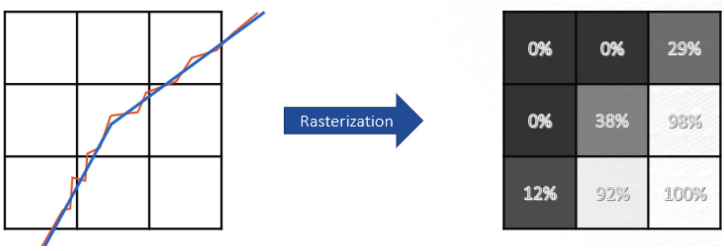


Figure 9. Rasterization of two different pixel dose equivalent input contours (red and blue) into a pixel grid, based on the pixel area coverage by the input contour.

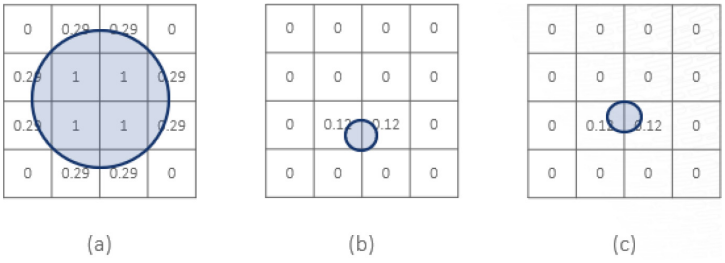


Figure 10. Rasterization of circles with different diameters and pixel alignments.

of how MBM writers would interpret the input data after the rasterization process. Figure 10 (a) shows a large enough circle that, ignoring other mask process effects, can be represented on the mask unambiguously. However, the examples from Figure 10(b) and Figure 10(c) show that different circles are rasterized to the same data in pixels and thus they are ambiguous. Here, the Nyquist rate and pixel sampling theory suggest that the pixel sizes are not sufficient to sample the data from Figure 10(b) and Figure 10(c). This issue would exist even if the masks undergo mask process corrections. The pixel size is generally fixed for a mask writer. Therefore, the data defining the mask shapes are bounded by the information theory.

ILT Computes the Mask by Evaluating Wafer Quality in Pixel Domain

The information content is also limited when considering how ILT simulates iteratively to generate the desired mask shapes that optimize for wafer performance. ILT performs lithography simulation of the mask using Fast Fourier Transforms, which is done in the pixel domain. Input curve defining the ILT mask is passed through a wafer simulation engine to generate the output curve as shown in Figure 11. For the user or the application engineer, the external behavior of ILT looks like the edges of polygons (either piecewise linear or curvilinear format) are being manipulated to generate the mask shapes. But the back-end calculations involve rasterizing the mask contour and using Fourier domain calculations for wafer simulation, which then gets contoured, to create the simulated contour. The simulated contour is then checked against the target, for validation, and sent to the mask shop after validation.

The ILT software needs to run as fast as possible, and as accurately as possible. Smaller grid sizes take longer to compute, so all ILT tools use sufficiently small, but large enough pixel sizes for computation, as dictated by the resolution of the wafer writing process, principally limited by the lithographic step, EUV or 193i, and the resist used for wafer processing. In either case, the smallest circle that can be represented reliably across all pixel-grid alignments is also a function of this pixel size. Thus, Pixel-Based Computing limits the information content in ILT computations too.

Information Theory in Mask Processing Data Flow

An ILT/OPC shop needs to follow mask rules prescribed by their mask shop. The mask shop, in turn, is expected to accurately print the mask as determined by ILT/OPC, so long as the mask rules are followed. ILT/OPC shop is essentially saying "please produce this mask as described because we verified that wafer performance will be best if you could manufacture this mask." And the mask shop's challenge becomes manufacturing the specified mask shapes on the physical mask as close as possible to the described shapes.

In the VSB era, a further approximation was implied in this collaboration agreement between the ILT/OPC shop and the mask shop. Because 90-degree corners (or any sharp corners for that matter) are known not to be manufacturable, ILT/OPC shops made assumptions about "corner rounding" that the mask shapes would suffer. Because of limitations in computational time, corner rounding is done in simple rule-based approximations. An exact mask process may not be known at the time of ILT/OPC also, making any simulation-based methods inaccurate anyway. Furthermore, the corners have significantly worse dose margins on the mask as compared to straight edges in VSB writing. This makes the corner rounding different for different instances of corners, even if the corners belong to the same overall shapes in different locations across the mask. This practice is fine for lightly OPC'ed shapes because the precision of those corners is not that important to overall circuit performance, even if the errors are transmitted to the wafer. But it is increasingly a problem for heavily decorated OPC or Manhattanized ILT, as the corners are close to each other with small jogs of 20nm occurring often in the mask shape. Since 20nm is well below the three sigmas of the blur radius of the mask process, the error induced by "corner rounding" can be very significant. And dose margin is effectively bad everywhere on these shapes.

Curvilinear shapes, most specifically, manufacturable curvilinear shapes fix this problem. Wafer simulation done in the ILT/OPC shop to certify the mask to produce good wafer performance is now simulating a mask that can actually be manufactured. Further, and perhaps much more importantly, these masks have a much more uniform dose margin across all shape edges. Manufacturable shapes are more reliably manufacturable. 90-degree corners are not manufacturable.

Not by accident, the MBM writers all have pixel resolution of the mask writers smaller than the resolution of 193i or EUV (at 4x dimensions), and therefore the resolution used by Curvilinear ILT in computing wafer images during ILT iterations. This does not by itself guarantee that all Curvilinear ILT outputs are inherently manufacturable on MWM writers. But it does make it

much more likely and therefore reduce significantly the amount of adjustments needed to obey MRC rules as prescribed by the mask shop.

Nevertheless, it is critically important for the mask shop to be provided with a sufficiently exact specification of the mask shapes that must be produced to preserve the wafer quality achieved by the ILT/OPC shop. The mask writer must be provided the shapes to write, and inspection, metrology, and repair tools need to know the shapes to compare with. Of debate is how much information is sufficient to exactly represent the information content assumed during ILT/OPC.

Demanding precise contour Edge Placement Error (EPE) at infinite resolution is enticing but it is not necessary. What is more important is pixel dose equivalence at wafer simulation. The data is sampled into pixels in two ends. First, in the wafer simulation software with ILT grid and then, in the mask writer using multi-beam pixel size. The data sampling during these two steps would act like low pass filters that make the notion of exact contour irrelevant and thus make contour-based EPE checks somewhat insufficient and misleading in the 2-D curvy region.

So reliably transferring the dose information to the mask is important. Mask writer only cares about the dose that it needs to project at every pixel. Any more data will be lost in the low-pass filtering process as depicted in figure 9. Transferring anything less is inaccurate and anything more is wasteful.

Conclusion

OPC/ILT that generates the mask shapes as well as the mask writer both uses pixels in some part of the data path. Pixel-based computing adds a low-pass filter to data processing. So, in summary, we can say information theory bounds all mask computations. The information beyond what OPC/ILT uses is irrelevant as the information used by ILT is sufficient for the wafer quality. The information beyond what MBM writers can write is wasted as it cannot be interpreted by the writer.

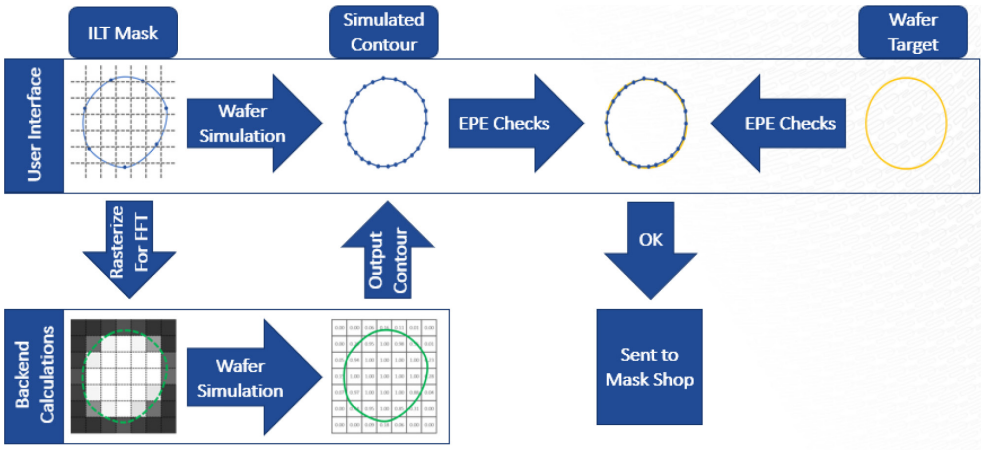


Figure 11. ILT mask validation process.

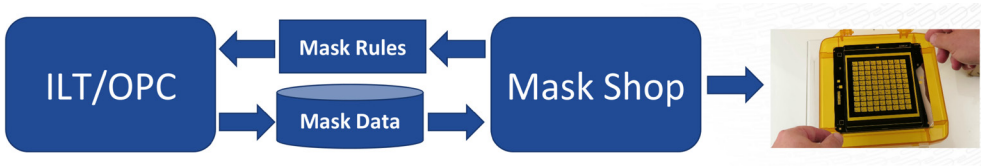


Figure 12. Collaboration between the ILT/OPC shop and mask shop.

As shown in Figure 14, it does not matter whether the red piecewise linear contour was used to define the mask, or the dark blue piecewise curvilinear contour was used. The multi-beam writer will rasterize both these contours in the same way, and they get translated to the same pixel values. So, the amount of dose projected on a mask is the same. Thus, by construction, it will produce the same mask. That is why pixel dose equivalence is sufficient and oversampling is just an unnecessary burden to the data path.

$$\text{Maximum number of vertices required} \approx \left(\frac{\text{contour perimeter}}{\text{pixel size}}\right)$$

We need enough information to accurately represent the area coverage of the pixel. So, having a maximum vertex count roughly in the order of contour perimeter over pixel size is sufficient to have pixel dose equivalence.

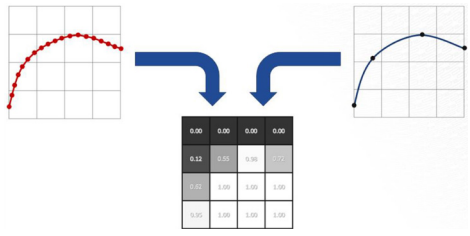
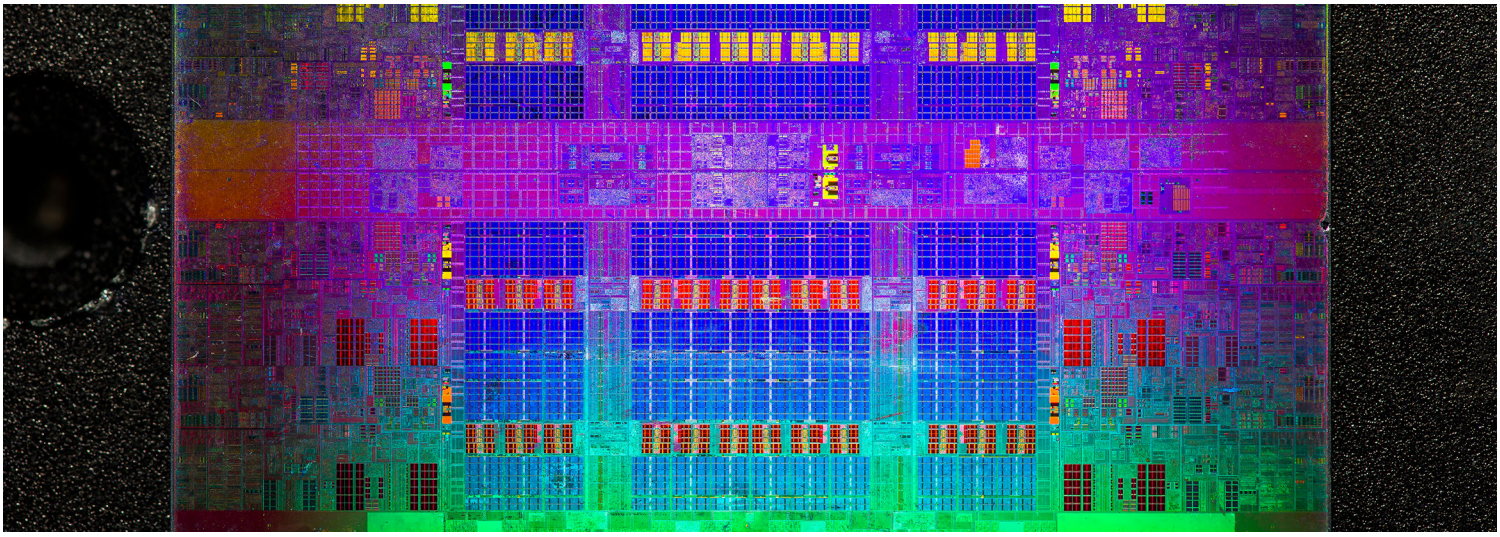


Figure 13. Example showing pixel dose equivalence is sufficient.

It is certainly possible to represent some curves using a lesser number of vertices. For example, a circle can just be represented using its center and radius irrespective of its size or perimeter. Therefore, equation (4) represents the maximum number of effective vertices required for tighter curves that still satisfy all the constraints of information theory and Nyquist rate. For a mask writer with a 16nm pixel, this is roughly 16nm on a mask or 4nm on a wafer. So, we do not need a 1nm segment polygon to represent the mask. Here 1nm is just a metaphor for oversampling. Yes, it is necessary to know the exact contour desired by ILT for the mask writer as well as for inspection and metrology tools. Representing the curve with segments that accurately interprets the desired curvy target, using a sampling interval in the order of multi-beam writer pixel size should be more than sufficient. Having a curvy representation that is pixel-based computing aware and using pixel-based computing in MDP will help keep the file size small while maintaining information integrity and thus the quality of the masks written by multibeam mask writers.

REFERENCES



1 Matsumoto, H., Inoue, H., Yamashita, H., Morita, H., Hirose, S., Ogasawara, M., Yamada, H. and Hattori, K., "Multi-beam mask writer MBM-1000 and its application field," Proc. SPIE 9984, Photomask Japan 2016: XXIII Symposium on Photomask and Next-Generation Lithography Mask Technology, 998405 (10 May 2016).

2 Pang, L., "Inverse lithography technology: 30 years from concept to practical, full-chip reality," J. Micro/Nanopattern. Mats. Metro. 20(3) 030901 (31 August 2021).

3 Pearman, R., Shendre, A., Syrel, O., Zable, H., Bouaricha, A., Niewczas, M., Su, B., Pang, L. and Fujimura, A., "Full-chip GPU-accelerated curvilinear EUV dose and shape correction", Proc. SPIE 10451, Photomask Technology 2017, 1045108 (31 October 2017).

4 Choi, J., Ryu, S., Lee, S., Kim, M., Lee, S., Buck, P., Durvasula, B., Gharat, S. and Liubich, V., "Status of curvilinear data format working group", Proc. SPIE 12325, Photomask Japan 2022: XXVIII Symposium on Photomask and Next-Generation Lithography Mask Technology, 1232508 (15 September 2022).

5 Pang, L., Russell, E., Baggenstoss, B., Lu, Y., Lee, M., Digaum, J., Yang, M., Pearman, R., Ungar, J., Sha, L., Bouaricha, A., Pomerantsev, M., Niewczas, M., Wang, K., Su, B., Meyer, M. and Fujimura, A., "Enabling faster VSB writing of 193i curvilinear ILT masks that improve wafer process windows for advanced memory applications," Proc. SPIE 11518, Photomask Technology 2020, 115180W (7 October 2020).

6 Shannon, C., "A mathematical theory of communication," in The Bell System Technical Journal, vol. 27, no. 3, pp. 379-423 (July 1948).

7 Shannon, C., "Communication in the Presence of Noise," in Proceedings of the IRE, vol. 37, no. 1, pp. 10-21 (January 1949).

8 Nyquist, H., "Certain Topics in Telegraph Transmission Theory," in Transactions of the American Institute of Electrical Engineers, vol. 47, no. 2, pp. 617-644 (April 1928).

9 Calma Corporation, GDS II Stream Format (July 1984).

10 OASIS - Open Artwork System Interchange Standard; P39-0304E2, SEMI - Semiconductor Equipment and Materials International. (2002).

11 Reich, A., Nakagawa, K. and Boone, R., "OASIS vs. GDSII stream format efficiency," Proc. SPIE 5256, 23rd Annual BACUS Symposium on Photomask Technology, (17 December 2003).

12 Abboud, F., Asturias, M., Chandramouli, M. and Tezuka, Y., "Mask data processing in the era of multibeam writers", Proc. SPIE 9235, Photomask Technology 2014, 92350W (21 October 2014).

13 Zable, H., Matsumoto, H., Yasui, K., Ueba, R., Nakayamada, N., Shirali, N., Masuda, Y., Pearman, R. and Fujimura, A., "GPU-accelerated inline linearity correction: pixel-level dose correction (PLDC) for the MBM- 1000," Proc. SPIE 10454, Photomask Japan 2017: XXIV Symposium on Photomask and Next-Generation Lithography Mask Technology, 104540D (13 July 2017).

14 Matsumoto, H., Yamaguchi, K., Kimura, H. and Nakayamada, N., "Multi-beam mask writer, MBM-2000," Proc. SPIE 11908, Photomask Japan 2021: XXVII Symposium on Photomask and Next-Generation Lithography Mask Technology, 119080L (23 August 2021).

15 "LEF/DEF Language Reference" Product Version 5.8, May 2017, Cadence Design Systems, coriolis.lip6.fr/doc/lefdef/lefdefref/lefdefref.pdf.

16 "Confidence in Curvilinear Mask Making Remains High", page 15, "2022 eBeam Luminaries Survey", www.ebeam.org/docs/2022-ebeam-luminaries-survey-final-1.pdf (2022) Proc. of SPIE Vol. 12293 1229307-11.

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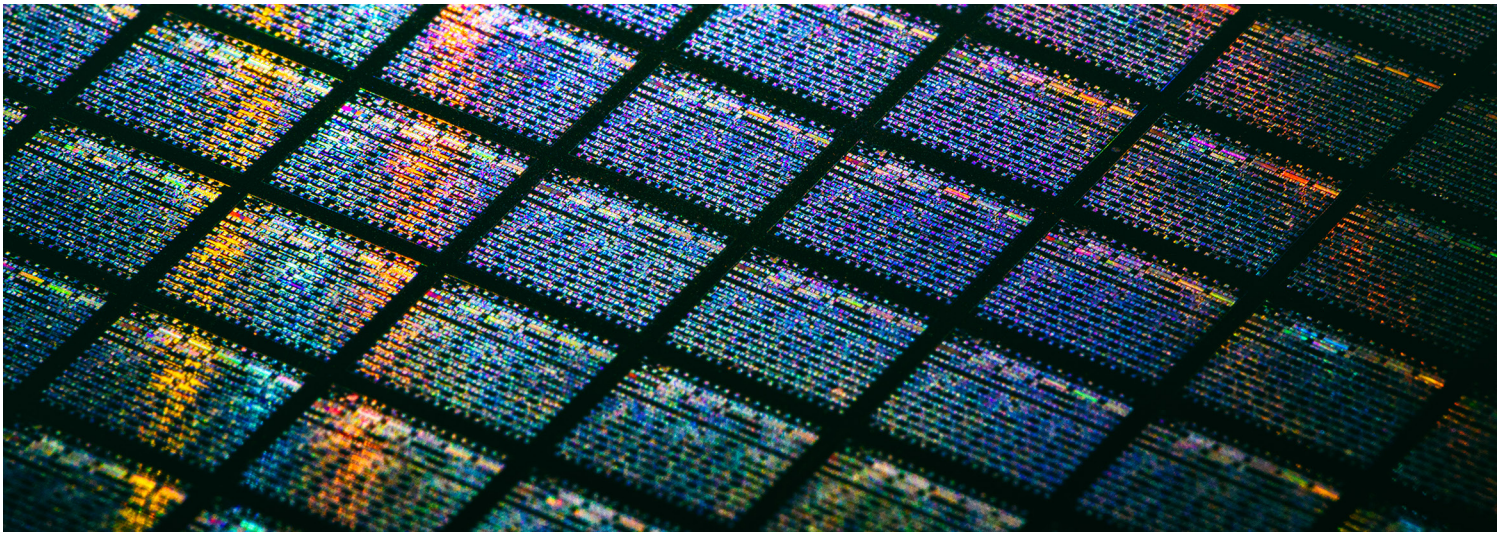

Global top ten foundries revenue grew 6% in 3Q22

Joanne Chiao & Eden Chung, *TrendForce*

The global top ten foundries total revenue grew 6% sequentially to $35.21 billion for 3Q22 but is expected to enter a correction period in 4Q22. The top 5 foundries were led by TSMC, followed by Samsung, UMC, GF and SMIC with a collective market share of 89.6%. TSMC saw revenue grow 11.1% sequentially driven by 7nm and below nodes.

https://www.trendforce.com/presscenter/news/20221208-11495.html

Japan to focus on next generation semiconductors

Allen Hsieh & Adam Hwang, *Digitimes*

Japan is focusing on next generation semiconductors, according to Hashimoto Kazuhito, president of Japan Science and Technology Agency, which is Japan's national R&D agency. The US leads in IC design, Taiwan leads in wafer foundry and IC packaging/test and South Korea leads in DRAM/flash so Japan is focusing on expertise in other areas such as compound and optical semiconductors.

https://www.digitimes.com/news/a20221207PD206.html

Japan and the Netherlands are expected to join US effort to tighten chip control to China

Takashi Mochizuki et al., *Bloomberg*

Japan has agreed in principle to join US efforts to tighten controls over the export of advanced chipmaking equipment to China with an announcement coming in weeks that they and the Netherlands will adopt at least some of the US restrictions. A three country alliance could represent a near-total blockade of China's ability to buy equipment necessary for making leading-edge chips.

https://www.bloomberg.com/news/articles/2022-12-12/japan-is-said-to-join-us-effort-to-tighten-chip-exports-to-china?leadSource=uverify%20wall

TSMC constructing a second fab in Arizona

TSMC

TSMC confirmed that they have started construction of a second fab in Arizona scheduled to begin the 3nm production in 2026. The overall investment for the two fabs on site will be $40 billion.

https://pr.tsmc.com/english/news/2977

YMTC the first to 200+ layer NAND flash

TechInsights

YMTC's Xtacking 3.0 technology is reported to be the first company to achieve a 200+ layer 3D NAND flash solution in the market, placing YMTC as the market leader in NAND flash technology.

https://www.techinsights.com/disruptive-event/ymtc-232l-tlc-3d-nand

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2023

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San Jose, California, USA
www.spie.org/al

SPIE Photomask Technology and EUV Lithography
1–5 October 2023
Monterey, California, USA
www.spie.org/puv

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19–21 June 2023
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