High sensitivity repeater detection with broadband plasma optical wafer inspection for mask defect qualification

Andrew Cross, Kaushik Sah, Vidyasagar Anantha, Balarka Gupta, Ramon Ynzunza, Neil Troy, Kenong Wu, Raghav Babulnath, Meghna Rajendran, KLA Corporation, One Technology Drive, Milpitas, CA 95035, U.S.A.

Dieter Van den Heuvel and Philippe Leray, Imec, Kapeldreef 75, 3001 Heverlee, Belgium

ABSTRACT

As extreme ultra-violet (EUV) lithography moves into high volume manufacturing (HVM) for several critical layers for the N5 node, there is a need to develop a comprehensive strategy for mask re-qualification in the fab to mitigate contamination risks. The introduction of additional particle sources due to the scanner vacuum system and potential growth of film or particle deposition on the reticle, in combination with pellicle uncertainty, pose unique inspection challenges for EUV reticle defectivity compared to 193i reticles.

EUV reticles are typically inspected with optical reticle inspection tools at outgoing quality control during their manufacture. Optical reticle inspection tools are also traditionally used in the IC fab for incoming reticle qualification and periodic reticle re-qualification during production. However, to reduce material at risk in the IC fab there is a need for alternate inspection methodologies based on inspection of printed wafers. In addition, potential new defect mechanisms, such as those associated with the multi-layer mask of the EUV reticle, are driving fabs to re-qualify reticles in production using new methods that involve printed wafer inspection. The printed wafer inspection methodology is referred to as “reticle print check” or simply “print check”. In this paper we will describe the print check flow and show results from new developments in this methodology improving the capture of mask defects on wafer.

Figure 1. Print check flow.
Positive Prospects for the Photomask Market with a Few Curves Ahead

Aki Fujimura, CEO, DS2

The 2020 editions of the two annual surveys conducted by the eBeam Initiative reflected optimism in our community about long-term opportunities and the short-term business impact due to COVID-19. These surveys include the Mask Makers survey, which covers the statistical facts about the masks made in the last year, and the Luminaries survey, which gathers opinions from industry luminaries about where they think the industry and its technologies are going. While COVID-19 introduced challenges to global markets overall, the sentiment among key decision makers within the photomask market segment remains neutral or positive about the growth in 2021 according to the Luminaries survey, completed in July 2020.

In semiconductor manufacturing, the move to EUV for critical layers of leading-edge nodes, the proliferation of multi-beam mask writers, and the emergence of curvilinear mask shapes provide a lot of excitement and opportunities for the year ahead. Multi-beam mask writing has been in production use for a few years now. EUV for wafer lithography has entered production use and is seeing a high rate of innovation throughout the manufacturing process. Among the results of the 2020 Mask Makers survey, the number of masks written with multi-beam writers more than doubled versus last year’s survey while EUV mask yield was reported at 91 percent.

Deep learning continues to be a topic of debate in semiconductor manufacturing. In the 2020 Luminaries survey, we asked a question on that subject. About two thirds of the people responding believe that deep learning will be deployed somewhere in the mask making process by 2022. Some thought that maybe sometime in 2023, and some thought it would never be used. The opinions are not as uniform as if you had asked “would deep learning be deployed in autonomous driving?”

My personal thought is that deep learning will start to get deployed in mask making soon. Just to reiterate, deep learning is a particular version of machine learning. Machine learning prior to deep learning is already being used, particularly in analyzing big data. But deep learning enables a whole new set of possibilities for helping to manufacture better and faster. For example, in the process of doing inverse lithography technology (ILT), you can speed up the processing quite a bit, around 2x or more. It can also improve accuracy by making fast estimations of effects that would otherwise be too computing intensive to incorporate. Multiple papers have been published on the use of deep learning for the mask 3D effect compensation, for example. In addition, because deep learning is so involved in image processing, applications that automatically analyze SEM images or automatically categorize defects detected by inspection will be deployed in mask shops. Deep learning has a trap in that it is easy to prototype but requires tremendous amount of data to make it production quality. Just as the autonomous driving community has found, digital twins that generate data, like an image of a child plastics part of a particularly tricky type of a defect, are critical. You don’t need them for a prototype to show promising results. You just must have them for production deployment of deep learning.

Most respondents to the 2020 Luminaries survey predict that some leading-edge masks will have at least some curvilinear shapes on them by 2023. The Mask Makers survey hasn’t tracked any data on the use of curvilinear shapes yet. In 2021, we should start to see at least some experimentation with curvilinear mask shapes being produced in mask shops and would be a good time to add this to the Mask Makers survey. Curvilinear mask shapes are desirable for improving resilience to manufacturing variation in wafer production. However, prior to production availability of multi-beam mask writing, it wasn’t practical to write curvilinear mask shapes with the traditional variable-shaped beam (VSB) writers. With multi-beam mask writers removing this constraint, and with ever increasing demand for precision on the wafer to improve process windows, curvilinear mask shapes are desirable for both 193i lithography and EUV lithography. Some unique aspects of reflective masks in EUV add to the need for curvilinear shapes on EUV masks. In addition, for other reasons, EUV masks need to be written on multi-beam mask writers anyway, so there is no barrier to using curvilinear shapes.

With the write-time barrier solved thanks to the multi-beam writers, defining and manipulating curvilinear mask shapes now becomes an opportunity for ILT, a technique that computes the desired mask shapes in order to maximize the quality of wafer lithography. Until recently, ILT faced the problem of long runtimes. Fortunately, the incredible advances in graphic-processing units (GPUs) solves this problem. The latest NVIDIA ‘Ampere’ series of processors provide around 20 TFLOPS (tera-floating operations per second) with 7,000 to 10,000 cores using 7-nm full-reticle designs. Just as multi-beam writing using pixels makes mask writing speed independent of shape complexity, GPU-based algorithms are pixel-based, making compute time independent of shape complexity.

Like the luminaries reflected in the survey taken in July 2020, I am optimistic about 2021. Perhaps the debate on deep learning will be answered through evidence of clear product differentiation. We should see more validation of multi-beam and EUV in the 2021 surveys and it’s time to start tracking when photomasks are curvilinear.
For our experiments, we used a BEOL M1 multi-die mask with a foundry (back end of line) logic type mask and simple litho stack. The reticle print check inspection methodology has been developed over the past few years. During this time, the unique capabilities required on the optical patterned wafer inspection tool were characterized, and the print check monitor itself was optimized to maximize sensitivity. The typical print check flow can be seen in Figure 1 where dedicated wafers are printed for optical defect inspection and SEM review. Due to multiple noise sources from previous patterning layers, short-loop wafers are preferred in this flow as our goal is to detect current layer mask defects with maximum sensitivity. In the wafer print check flow wafers are inspected at ADI (after develop inspection) to reduce cycle time.

Several factors have been identified as being critical to maximizing the sensitivity of print check inspection. Figure 2 shows the concept of signal-to-noise ratio for a wafer inspection system. In order to detect a defect, an inspector must use source (illumination), optical, detector (sensor) and algorithm subsystems that maximize signal from the defect and minimize overall noise. To meet sensitivity requirements for print check applications at the N5 node achieving a sufficient signal-to-noise ratio needs to be considered. Inspection tool choice is one of the most critical factors for print check inspection as chipmakers are looking for high sensitivity coupled with the throughput needed to support production use cases. KLA’s broadband plasma (BBP) wafer inspection technology platforms leverage a 190-260nm inspection wavelength range to provide high sensitivity for a variety of critical EUV defect types at ADI with acceptable throughput for HVM. Sensitivity has been validated with simulations and numerous empirical studies.

Another factor critical for print check inspection sensitivity is the litho stack. Further defect signal improvement may be achieved by using simulations to identify optimal (but compatible) underlying films used in the litho stack. This is possible as print check is typically implemented as a monitor methodology on dedicated wafers. This optimization is described as stack engineering. Benefits of such an optimization to improve sensitivity are discussed in previous publications.

Finally, new inspection capabilities and algorithms have been developed to improve signal to noise ratio through reduction of systematic and random inspection noise for both single die reticle and multi die reticle use cases. This paper emphasizes these noise reduction capabilities that significantly improve sensitivity on KLA’s 392x inspection platforms. The complete print check flow is implementation on a KLA/IMEC IN7 BEOL (back end of line) logic type mask and simple litho stack.

**INTRODUCTION**

The reticle print check inspection methodology has been developed over the past few years. During this time, the unique capabilities required on the optical patterned wafer inspection tool were characterized, and the print check monitor itself was optimized to maximize sensitivity. The typical print check flow can be seen in Figure 1 where dedicated wafers are printed for optical defect inspection and SEM review. Due to multiple noise sources from previous patterning layers, short-loop wafers are preferred in this flow as our goal is to detect current layer mask defects with maximum sensitivity. In the wafer print check flow wafers are inspected at ADI (after develop inspection) to reduce cycle time.

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**EXPERIMENT AND RESULTS**

For our experiments, we used a BEOL M1 multi-die mask with a foundry N7 equivalent design. The M1 layer was printed with EUV single patterning on a simple litho stack as shown in Figure 3. We designed programmed defects in one of the dies of the mask. These programmed defects, or PDs, can help us to demonstrate sensitivity improvements in the absence of actual adders on the mask, especially when the mask is new, and to remove the uncertainty of when an adder may be added. The mask layout and examples of a few programmed defects are shown in Figure 4. Optical inspections and SEM review were done on KLA’s 392x broadband plasma optical patterned wafer inspector and eDR7380™ e-beam review system. A reticle print check itself was optimized to maximize sensitivity. The print check monitor was implemented with an automated sensor (SOG) of 392x and eDR7380™ e-beam review system.

Figure 5 shows the SNR challenges for small programmed defects at ADI. As already discussed and has been shown in previous work, ensuring that the inspection platform provides signal to the defect of interest is essential. The 392x brings unique capabilities for ADI inspection, with regards to its optical source, flexible modes and existing algorithms.

We can see that even if signal is clear on the optical inspection images from 392x, noise sources throughout the wafer leads to low or barely detectable defects (low SNR). In other words, signal from small defects are often buried into the noise and this presents a problem in their reliable detection. Noise sources as seen by the optical inspector can be broadly categorized into systematic and random noise categories. Systematic noise can be design related (i.e. certain structures are inherently noisier) or process related, such as film thickness variations or CD (critical dimension) variation, which is perceived as contrast or color noise. Then there are random noises which come from pattern fidelity such as high LER (line edge roughness) and LDCU (local CD uniformity). Some of the examples of these noise sources are shown in Figure 6.

To be precise, when we talk about noise as seen by the optical inspection tool, we refer to gray level variations in the defect difference image. This variance can be measured as one-sigma value to quantify this noise impact. With algorithmic and platform improvements in defect detection capabilities, noise can be significantly reduced to increase SNR. The result of these improvements is clear when we compare the standard deviation image with that obtained from new print check algorithms.

The reduction in noise is seen for both systematic and random structures as shown in Figure 7. This leads to significant improvement in SNR as shown in Figure 8, leading to reliable capture of repeater defects that would be barely detectable otherwise.

With an inspection recipe implementing these new capabilities for print check, inspection of a reticle row was done, and results compared to standard die-to-die inspection recipe with the same optics parameters and nuisance rate. The comparison was done in terms of programmed repeater locations identified by both inspections. Figure 9 shows the comparison results split by programmed repeater type, grouped into resist add type defects (or resist bridges) and resist missing type defects (or resist opens).

As seen, print check inspection captures 2.5 times as many repeater defects as shown in figure 8, leading to reliable capture of repeater defects that would be barely detectable otherwise.

Finally, new inspection capabilities and algorithms have been developed to improve signal to noise ratio through reduction of systematic and random inspection noise for both single die reticle and multi die reticle use cases. This paper emphasizes these noise reduction capabilities that significantly improve sensitivity on KLA’s 392x inspection platforms. The complete print check flow is implementation on a KLA/IMEC IN7 BEOL (back end of line) logic type mask and simple litho stack.
Figure 4. a) Mask layout showing 3x1 identical dies with programmed defects in middle die; b) add or cut type examples of programmed defects.

Figure 5. Examples of resist missing defects showing SNR challenges. Suppressing the noise is desirable to increase SNR.
CONCLUSIONS

In this paper we discussed the reticle print check inspection methodology to monitor EUV mask defects. Optical inspection is currently the only method to provide the coverage and throughout required for this use case. Having high defect detection sensitivity at HVM throughputs is one of the most critical steps in the print check flow. In order to maximize sensitivity and reduce unwanted noise, we recommend the use of short loop ADI monitoring wafers. We discussed various noise sources as seen by an optical inspector coming from the wafer. In order to increase sensitivity for challenging defects, it is imperative that the impact of these noise sources be minimized. To this end, new print check capabilities have been developed on KLA 392x platforms. They result in significant reduction in wafer noise and increased SNR. Experimental data was shown demonstrating considerable improvement in capture of programmed repeater locations as compared to standard inspection with the same optical settings. In both inspections defect signals are similar, with the new capability providing significant improvements in both random and systematic noise sources. Further improvement in defect signal is possible by optimizing the litho stack via stack engineering\[3\]. In closing remarks, we would like to highlight that although in this paper we used a multi die reticle to evaluate the performance of print check algorithms, we are also evaluating the methodology for single die reticle use case.

Figure 6. Examples of various noise sources seen by the optical inspection system.

Figure 7. Reduction in noise with new print check capability (right). 1-sigma noise is much higher in standard difference image so much so that fingerprint of systematic structures can be clearly seen (center).
REFERENCES


[2] Ben Tsai, “Inspection and Metrology to Support the Quest for Perfection: photolithography for the Sub-10nm Nodes,” SPIE Advanced Lithography 2017


Figure 8. Improvement in SNR with noise suppression using print check algorithms.

Figure 9. Comparison between print check and standard inspection. Print Check algorithms captures about 2.5x repeater locations compared to standard inspections due to reduction in noise.
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■ There’s a global shortage of computer chips – what’s causing it?

Matthew Sparkes, New Scientist

The world is experiencing a computer chip shortage due to a perfect storm of problems including a global pandemic, a trade war, fires, drought and snowstorms. It has coincided with a period of soaring, unprecedented demand – in January alone, chip sales reached a record $40 billion. Chips are now in everything from watches to fridges and your car probably has several dozen. Manufacturers simply can’t produce them fast enough.


■ U.S. Must Fabricate High-End Chips Again [editorial]

John Neuffer, CEO of the Semiconductor Industry Association, letter to the Wall Street Journal

Your editorial “The Semiconductor Shortage” (March 13) is right that government action is not needed to correct the short-term supply-demand imbalance causing the global chip shortage, but wrong that the U.S. can “prod” its way to stronger domestic semiconductor production.

https://www.wsj.com/articles/u-s-must-fabricate-high-end-chips-again-11616098776?mod=searchresults_pos1&page=1

■ Race is on for used chipmaking equipment.

by Dave Makichuk, Asia Times

It’s an old expression — one man’s junk is another man’s treasure. You might say that’s the case with China’s semiconductor makers, who are snapping up used chipmaking machines as fast as they can buy them.

The surprising thing is where they’re getting them from — Japan. According to a report in Nikkei Asia, the rush to produce homegrown products in China amid US-Sino trade tensions is driving up equipment prices in Japan’s massive secondary market. Japanese used equipment dealers say prices are up by 20% from last year.

https://asiatimes.com/2021/03/the-race-is-on-for-used-chipmaking-equipment/

■ Darpa funds ASIC accelerators for fully homomorphic encryption

by Sally Ward-Foxton, EE Times

The US Defense Advanced Projects Agency (Darpa) has awarded contracts to four teams to develop ASIC accelerators for fully homomorphic encryption as part of its data protection in virtual environments (DPRIVE) program. The four contracts have been awarded to teams led by Duality Technologies, Intel, SRI International and Galois. Three of the four are worth between $11.5 million to $15 million; Intel did not disclose the amount of its award.

https://www.eetimes.com/darpa-funds-asic-accelerators-for-fully-homomorphic-encryption/

■ Manufacturing Bits: March 8: Two-beam EUV lithography; EUV SADP; dry resists

by Mark LaPedus, Semiconductor Engineering

At the recent SPIE Advanced Lithography conference, Nikon gave a presentation on a two-beam extreme ultraviolet (EUV) lithography technology. Still in the conceptual phase, Nikon’s so-called EUV Projection Optical Wafer Exposure Ruling Machine, or EUV Power Machine, is designed for the 1nm node or so. The proposed system has a minimum resolution of 10nm for lines and spaces in single patterning applications.

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  [www.photomask-japan.org](http://www.photomask-japan.org)

- **The 36th European Mask and Lithography Conference, EMLC 2021**
  22 June 2021
  Digital Event

- **SPIE Photomask Technology + EUV Lithography**
  26-30 September 2021
  [https://spie.org/conferences-and-exhibitions/puv](https://spie.org/conferences-and-exhibitions/puv)

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International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
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