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Mask Infrastructure | Mask Integration |
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Technical Program
Conferences + Courses: 13-16 September 2010
Exhibition: 14-15 September 2010
Monterey Conference Center and Monterey Marriott Hotel
Monterey, California, USA
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Welcome to Photomask!

On behalf of SPIE, BACUS, and the Conference Organizers, we would like to welcome you to attend the 30th Annual SPIE/BACUS Photomask Symposium. This continues to be the premier worldwide technical meeting for the photomask industry. This year’s symposium will give the authors an opportunity to present their exciting research findings that relate to the emerging technical challenges facing the photomask industry, to an international audience of their peers.

This year we will open on Tuesday with the Keynote Presentation by Dr. Franklin D. Kalk, Toppan Photomasks, titled The Future is Bright for Those with Open Eyes. Dr. Kalk will certainly have insight into the photomask industry, so you won’t want to miss his presentation!

We have received 150 presentations this year, so it should be a very informative week! The all-day Wednesday Special Session in on EBDW/ML2: 13.5 Nanometer or 17.3 Picometer?: not enough R&D $s to go around? From ‘Plenty, but Never Enough’ to ‘Badly Needed’: are we funding the right technology/wavelength? Our Co-Chairs Brian Grenon and Wolf Staud have solicited the contributions of industry luminaries on the various subjects and challenges that ML2 is facing: starting with Aki Fujimura, D2S, Inc. [Keynote Speaker], Hans Pfeiffer [historical background], Neil Berglund [CoO], David Lam, [Complementary Lithography], Tor Sandstrom [platform], Laurent Pain [datapath] and many more tool and sub-system suppliers to give you a great program on this more than viable alternative.

We welcome you to beautiful Monterey! Not only will you have a great experience attending the sessions, you can also plan on staying on for a few days in the City by the Bay!

---

**Conference Chair**

M. Warren Montgomery  
College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc.

**Conference Co-Chair**

Wilhelm Maurer  
Infineon Technologies AG (Germany)
Floorplans

Marriott Floorplan

Monterey Conference Center Floorplan
SPIE would like to express its deepest appreciation to the symposium chairs, conference chairs, program committees, session chairs, and authors who have so generously given their time and advice to make this symposium possible.

The symposium, like our other conferences and activities, would not be possible without the dedicated contribution of our participants and members. This program is based on commitments received up to the time of publication and is subject to change without notice.

Keynote Presentation

The Future is Bright for Those with Open Eyes

*Room: Steinbeck Forum*

Tuesday 14 September, 8:10 to 8:50 am

Franklin Kalk, Executive Vice-President, Technology Toppan Photomasks

Don’t miss this exciting opening Keynote on Tuesday morning.

Special Session on EBDW/ML2

13.5 nm or 17.3 Picometer? Are We Funding the Right Wavelength/Technology?

*Room: Steinbeck Forum*

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APPLIED MATERIALS

Wednesday 15 September • 8:00 am to 5:30 pm

See page 5.

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Keynote Presentation

The Future is Bright for Those with Open Eyes

Room: Steinbeck Forum
Tuesday 14 September • 8:10 to 8:50 am

Dr. Franklin Kalk is Toppan Photomasks’ executive vice president of Technology, with responsibility for the company’s global R&D programs. His recent interest is the effect of next generation lithography on semiconductor industry business models. He is widely published and holds 18 U.S. patents. He received a Ph.D. in Optics from the University of Rochester.

Don’t miss this exciting opening Keynote.

Poster Viewing

Room: Serra Ballroom
Tuesday 14 September · 6:15 to 7:45 pm
Wednesday 15 September · 10:00 am to 3:00 pm

Poster authors may set up their poster papers between 10:00 am and 4:00 pm on Tuesday and will leave them up until Wednesday afternoon. Authors will be present during the Poster Reception 6:15 to 7:45 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any papers not removed by Wednesday at 3:00 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3:00 pm.

Exhibition/Poster Reception

Room: Serra Ballroom
Tuesday 14 September · 6:15 to 7:45 pm

Poster Reception Hors d’Oeuvres
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Poster Reception Beer
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Symposium attendees and guests are invited to attend an Exhibition/Poster Reception on Tuesday evening in the Serra Grand Ballroom. The reception provides an opportunity for attendees to meet colleagues, network, view poster papers, and visit the exhibition booths. Refreshments will be served. Attendees are requested to wear their conference registration badges.

SPIE Green Initiative

As host to events that bring together scientists and engineers from around the globe, SPIE is committed to making our symposia as environmentally friendly as possible.

Ongoing efforts of SPIE include using non-disposable materials such as glass plates and metal flatware as often as possible, and encouraging facilities to donate surplus meals to soup kitchens. Many partnering facilities have robust recycling programs for paper, plastic, and aluminum products. SPIE continues to collaborate with venues, hotels, suppliers and the local Chambers of Commerce to assess and ease the conference’s environmental impact. SPIE is currently working to implement solutions from the Green Meetings Industry Council guidelines with a goal to take our environmental efficiency to a whole new level.

When at this event, SPIE encourages you to take advantage of recycling bins, to reuse towels at your hotel, and to carpool whenever transportation is required during your stay in Monterey.

Stay up to date with current practice in photomask engineering. Courses on E-beam, EUV, and Photomask fabrication & technology.

Details on page 18.
Okay. We all drank the EUV Kool-Aid. Now it is time to ensure our roadmap. The increasing cost of lithographic masks is raising concerns for future technology generations and the Semiconductor roadmap at large. Cost-per-design is another limiting factor in diminishing the number of prototype starts. The staggering overall cost of EUV lithography, combined with even higher blank and finished mask cost, is driving another nail into the coffin of the semiconductor progress. One could argue that EUV appears to be only of benefit to true high-wafer-volume-per-mask end-users, that can absorb the cost thru their wafer, chip and systems cost.

As a result, semiconductor manufacturers are beginning to look for ways to reduce or eliminate the need for masks altogether - mask-less lithography (ML2) is one such approach.

In a sense, one variation of mask-less lithography - Electron-beam direct-write tools - have been around for decades and are still successfully used in the semiconductor industry for rapid device development. Typically, EBDW tools operate at 50keV electron-beam energy and have excellent resolution capabilities. The only reason the tools are not widely used in production is their lack of throughput. Multibeam maskless lithography offers all the benefits of EBDW while resolving the volume problem by implementing a massive parallelization of electron beams.

Massively-parallel Mask-less Lithography contrary to EUV is an innovation on an evolutionary path that to a large extent-capitalizes on existing e-beam technology parts (e.g., source, lenses, wafer stage, beam software, magnetic shielding, and tool software). The main advantage of ML2 is the realization of pattern transfer through an array of several hundreds or thousands of individually addressable electron beams, thereby pushing the potential productivity from hours-per-wafer into the wafer-per-hour regime. Furthermore, several ML2 tools can be clustered on the floor space allocated for just one EUV scanner, potentially providing 100wph for the 22nm hp node, capitalizing on the advantage of using the same common infrastructure with the added benefit of redundancy in case of downtime related to for instance source, optics clean, defects, or general contamination problems.

Please join us for what will surely be a very challenging and interesting session. For presentation information, see pages 15-16.
### Daily Schedule

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**19–22 September 2011**

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Monterey Marriott & Monterey Convention Center

Monterey, California, USA

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Exhibit Guide

See the latest in:
- Electron-beam lithography
- EUV
- Metrology
- Lasers
- Nanotechnology
- Optical/laser microlithography
- Resist technology and processing
- Software
- Electronic imaging components

Exhibitor List *(Current as of 8/3/2010)*

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Exhibition Floor Plan

SPIE PHOTOMASK 2010
Monterey Conference Ctr
Monterey, California USA
September 14-15 2010

Poster Area

COFFEE AND
DESSERT AREA

Freight Door

Main Entrance

Portola Lobby
Registration Area
Advantest Corporation
3201 Scott Blvd, Santa Clara, CA, 95054
408/988-7700; fax 408/987-0680
info@advantest.com; www.advantest.com

New Product: CD-SEM advanced mask metrology tools enable accuracy in photomask manufacturing.

Advantest is the leading producer of automatic test equipment (ATE) for the semiconductor industry and a leading manufacturer of measuring instruments used in the design and production of electronic instruments and systems. The company also maintains a focus on R&D for emerging markets that benefit from advancements in nanotech and terahertz technologies. More information is available at www.advantest.co.jp Contact: Greg Self, EVP Marketing, g.self@advantest.com; a.gold@advantest.com, Director, Corporate Communications.

Carl Zeiss SMS GmbH
Carl Zeiss Promenade 10, Jena, Germany, 07745
49 36 4164 2563 info-sms@smt.zeiss.com; www.smt.zeiss.com/sms

New Product: PROVE Registration and Overlay Metrology System working with 193nm optics for superior resolution.

Carl Zeiss is a global supplier of metrology and manufacturing equipment for the semiconductor industry. Core expertise in light and electron optics, complemented by a femto-second laser technology form the foundation of a product portfolio comprising in-die metrology, actinic qualification, repair/tuning and monitoring of photomasks. Our advanced mask solutions empower our customers in the mask making industry to develop and manufacture zero defect photomasks with highest yields. Contact: Jim Polcyn, Director Sales and Field Operations, SMS-US, polcyn@smt.zeiss.com.

Corning Incorporated
1 Riverfront Plz, Corning, NY, 14831
607/974-9000; fax 607/974-8177 www.corning.com

New Product: Tropel UltraFlat: Non-contact flatness metrology for photomasks and photoblanks.

Corning Tropel Corporation is a leading manufacturer of non-contact metrology instrumentation designed specifically for the photomask industry. Our Tropel® UltraFlat™ product line measures photomasks and photoblanks at every stage of the manufacturing process. Substrates that have been, polished, coated, patterned, or have had pellicles mounted to them are measured in just seconds; providing flatness data to 6 nanometer uncertainty. Contact: Chris Lee, Product Line Manager, lee@corning.com; Dave Young, Marketing Communications, youngd@corning.com.

Gudeng Precision Industrial Co., Ltd.
9F No 2 Sec 4 Jhongyang Rd, Tucheng City, Taipei, Taiwan, 236
886 2 2268 9141; fax 886 2 2269 1943 sales@gudeng.com; www.gudeng.com


Gudeng Precision has been assisting customers to enhance their product yield and reduce their production cost by providing custom-made products with innovative design concepts. Presently, Gudeng Precision is the world’s leading photomask total solution provider and our product is widely accepted by customers around the globe. Contact: Iris Liu, Sales, IrisLiu@gudeng.com; Rick Tsai, Sales, RickTsai@gudeng.com. www.gudeng.com

Heidelberger Druckmaschinen AG
2807 Oregon Ct Ste E2, Torrance, CA, 90503
310/312-6071; fax 310/212-5254 sales@heidelberg-instruments.com; www.hiit.de

New Product: Heidelberg Instruments has developed many advancements on existing platforms.

Heidelberg Instruments is a world leader in design, development and manufacturing of advanced laser based maskless lithography systems for production of photomask, as well as laser direct imaging. Applications include: Micro and Nano technology, MEMS, Displays, Advanced Packaging, ASICS, Micro Optics, and many other related fields. Contact: Matt Price, Manager, Marketing and Technical Sales, mprice@hiit.de; Janette La Bella, Sales Associate, jlb@hiit.de.

Inko Industrial Corp.
695 Vaqueros Ave, Sunnyvale, CA, 94085
408/830-10401; fax 408/830-1055 sales@pellicle-inko.com; www.pellicle-inko.com

New Product: 193 DUV pellicle with minimized outgas.

INKO, a U.S. based company, manufactures a complete line of pellicles for applications ranging from ASIC production, high volume memory production. From broadband to I/G line to 248 nm/193nm DUV lithography. We have the right pellicles for your needs. Contact Joe Mac, Sales and Customer Service, jomac@inko.com.

KLA-Tencor
1 Technology Dr, Milpitas, CA, 95035
408/875-3000; fax 408/875-4144 info@kla-tencor.com; www.kla-tencor.com

New Product: Heidelberg Instruments has developed many advancements on existing platforms.

KLA-Tencor is a world leader in design, development and manufacturing of advanced laser based maskless lithography systems for production of photomask, as well as laser direct imaging. Applications include: Micro and Nano technology, MEMS, Displays, Advanced Packaging, ASICS, Micro Optics, and many other related fields. Contact: Matt Price, Manager, Marketing and Technical Sales, mprice@hiit.de; Janette La Bella, Sales Associate, jlb@hiit.de.

Mentor Graphics
8005 SW Boeckman Rd, Wilsonville, OR, 97070-7777
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Pozzetta Inc.
3121 S Platte River Dr, Englewood, CO, 80110
303/783-3172; fax 303/374-7342
customerservice@pozzetta.com; www.pozzetta.com

New Product: 156mm Solar Wafer Products.
Companies around the world trust Pozzetta to create secure environments for the handling, storage, and transport of photomasks, reticles, and wafers. Pozzetta will protect your valuable products from particles, ESD damage, outgassed components, and high costs.

RAVE LLC
430 S Congress Ave Ste 7, Delray Beach, FL, 33445
561/330-0411; fax 561/330-0647
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Technology driven equipment company with a long history of unique technical contributions to the Photomask Industry. RAVE’s talented team is recognized for development and on-time delivery of innovative, cost-saving process solutions. RAVE is now delivering the new 5th Generation Merlin™ 22nm production mask repair nanomachine & the revolutionary Rhazer™ haze removal system. RAVE’s fp650 femto-pulse laser tool continues to be the fastest, most efficient >45nm production mask repair system. Contact: Dave Lee, V.P. Sales & Marketing, David.Lee@ravenano.com.

Shin-Etsu MicroSi, Inc.
10028 S 51st St, Phoenix, AZ, 85044-5203
480/893-8898; fax 480/893-8637
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Shin-Etsu, the world’s No. 1 supplier of semiconductor silicon wafers and a leading supplier of essential electronic materials. Shin-Etsu’s product portfolio includes, photomask blanks, EB resists, pellicles, synthetic quartz, semiconductor advanced resists along with numerous specialized thermal interface materials. Contact: Edwin Nichols, Marketing Manager, enichols@microsi.com; info@microsi.com.

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Solid State Technology is the leading global authority on semiconductor and thin-film manufacturing, covering developments in process technologies, tools and materials, enabling innovation, and problem solving by senior management, engineers, process developers, and other decision makers within the chip making and allied industries. Contact: Diane Lieberman, Group Publisher, diane@pennwell.com; Karen Watkins, Regional Sales Manager, karenw@pennwell.com.

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XEI Scientific manufactures and sells the Evactron De-Contaminator, which uses a unique RF plasma source to make either oxygen or hydrogen radicals for downstream ashing of hydrocarbons. The device is compact and is easy to install and operate. Over 900 Evactron De-Contaminators have been used in electron microscopes around the world. The process has been proven safe and effective for removing carbon contamination from EUV optics. Contact: Chrisopher G. Morgan, Product Manager, gabe@evactron.com; Vince Carlino, Sales Director, sales@evactron.com.

XYALIS  #307
World Trade Center Grenoble BP 1510, Grenoble, France, 38025
33 476 706 475
info@xyalis.com; www.xyalis.com
New Product: GTmask – Automated Mask Set generation warranting compatible mask sets between different equipments.
XYALIS is an EDA company offering a fully integrated Mask Data Preparation solution to eliminate the risk of error, reduce time to manufacturing, and increase manufacturing yield by automating frame generation, Multi-Project Wafers assembly, intuitive mask set creation, and wafer map optimization, and by streamlining the mask order process. XYALIS’ solutions have been developed in cooperation with major semiconductor industry leaders and have been used in production for years. Contact: Sylvie Hurat, US Area Manager, sylvie@xyalis.com.

Product Categories

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Displays
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Distributor or Reseller
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- Nippon Control System Corp.
- Plasma-Therm LLC
- Synopsys
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- Advantest Corporation

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- Mentor Graphics
- Plasma-Therm LLC
- Shin-Etsu MicroSi, Inc.
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- Advantest Corporation

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## Photomask Technology

**Conference Chair:** M. Warren Montgomery, CNSE/SEMATECH  
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### Tuesday 14 September

#### Opening Remarks

Session Chairs: M. Warren Montgomery, CNSE/SEMATECH; Wilhelm Maurer, Infineon Technologies AG (Germany)

8:10 am: *The Future is Bright for Those with Open Eyes (Invited Paper)*, Franklin D. Kalk, Toppan Photomasks, Inc. (United States) ............................................. [7823-01]

8:50 am: *Mask Industry Assessment: 2010*, Gregory P. Hughes, David Y. Chan, SEMATECH North (United States) ............................................. [7823-02]

9:10 am: *EMCL 2010 Best Paper: E-beam induced EUV photomask repair: a perfect match*, Markus Wablinger, K. Kornilov, Thorsten Hofmann, Klaus Edinger, Carl Zeiss SMS GmbH (Germany) ............................................. [7823-03]

9:30 am: *PMJ 2010 Best Paper: Dry etching technologies for EUV mask*, Tomaoki Yoshimori, Hirotsugu Ita, Yoshinori Iino, Hidehito Azumano, Mikio Nonaka, Shibaura Mechatronics Corp. (Japan) ............................................. [7823-04]

9:50 am: *PMJ 2010 Panel Overview (Presentation Only)*, Yoshinori Nagoaka, KLA-Tencor Japan (Japan); Shinji Akima, Toppan Printing Co., Ltd. (Japan); Hiroshi Mohri, Dai Nippon Printing Co., Ltd. (Japan); [7823-05]

Coffee Break ............................................. 10:10 to 10:40 am

### SESSION 5

**Room:** Ferrante ............................................. Tues. 11:00 am to 12:00 pm

**Session Chairs:** Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Douglas J. Resnick, Molecular Imprints, Inc.

11:00 am: *Development of template and mask replication using jet and flash-imprint lithography*, Douglas J. Resnick, Cynthia B. Brooks, Kosta S. Selinidis, Gary F. Doyle, Dwayne L. LaBrake, S. V. Sreenivasan, Molecular Imprints, Inc. (United States) ............................................. [7823-23]

11:20 am: *6-inch circle template fabrication for patterned media*, Morihisa Hoga, Kimio Itou, Dai Nippon Printing Co., Ltd. (Japan); Nobuhiro Toyama, Dai Nippon Printing Co. America, Inc. (United States) ............................................. [7823-24]

11:40 am: *Inspection technique for nano-imprint template with mirror electron microscopy*, Tomokazu Shinmura, Masaki Hasegawa, Hiroshi Suzuki, Hiroya Ohta, Hitachi, Ltd. (Japan) ............................................. [7823-25]

Lunch/Exhibition Break ............................................. 12:00 to 1:20 am

### Authors and Presenters

- Find full instructions for a successful presentation at Photomask Technology—oral and poster.
- Find full instructions for a successful manuscript preparation.
Tuesday September 14 (continued)
Sessions 2, 3, 4 run concurrently with sessions 5, 6, 7, 8.

SESSION 3
Room: Steinbeck Forum .......... Tues. 1:40 to 4:30 pm
Mask Process
Session Chairs: Emmanuel Rausa, Plasma-Therm LLC; Chin-Hsiang Lin Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)
1:40 pm: Process window improvement on 45-nm technology nonvolatile memory by CD uniformity correction. Ute Bertzger, Robert Birker, Carl Zeiss SMS GmbH (Germany); Erez Graitzer, Avi Cohen, Carl Zeiss SMS GmbH (Israel); Benedetta Trulini, Carmelo Romeo, Numonix Agrate (Italy). [7823-11]
2:00 pm: Degradation of pattern quality due to strong electron scattering in EUV mask. Jin Choi, Sang Hee Lee, Hee Bom Kim, Byung-Gook Kim, Sang-Gyun Woo, Han-Ku Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of). [7823-12]
2:20 pm: Reduced basis method for source mask optimization. Jan Pomplun, Konrad-Zuse-Zentrum für Informationstechnik Berlin (Germany) and JCMwave GmbH (Germany); Lin W, Zschiedrich, JCMwave GmbH (Germany); Sven Burger, Frank Schmidt, Konrad-Zuse-Zentrum für Informationstechnik Berlin (Germany) and JCMwave GmbH (Germany); Jacke K, Timynski, Nikon Precision Inc. (United States); Donis G, Flagello, Nikon Research Corp. of America (United States); Toshihuru Nakashima, Nikon Corp. (Japan). [7823-116]
2:40 pm: Plasma monitoring of chrome dry etching for mask making. Sung-Won Kwon, Dong-Chan Kim, Dong-Seok Nam, Sang-Gyun Woo, Han-Ku Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of). [7823-14]
3:00 pm: Long-range proximity effects and CD variation: a method to characterize chemical flare and develop loading. Linda K. Sundberg, Gregory M. Wallraff, Alexander M. Fritz, Blake W. Davis, IBM Almaden Research Ctr. (United States); Amy E. Zwebner, IBM Corp. (United States); Emmanuel Delamarche, Robert D. Lovchik, IBM Zürich Research Lab. (Switzerland); William D. Hinsberg, IBM Almaden Research Ctr. (United States). [7823-15]
3:50 pm: New method to determine process window considering pattern failure. Shinzo Hasegawa, Sung-Ki Kim, Sung-Chul Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of). [7823]
4:10 pm: A systematic approach to the determination of SRAF capabilities in high-end mask manufacturing. Christian Buergel, Martin Sczybyra, Advanced Mask Technology Ctr. GmbH Co. KG (Germany). [7823-17]

SESSION 4
Room: Steinbeck Forum .......... Tues. 4:30 to 6:10 pm
Mask Materials
Session Chairs: Mark T. Lee, HOYA Corp. USA; Thomas B. Faure, IBM Corp.
4:30 pm: Development and characterization of a thinner binary mask absorber for 22-nm node and beyond. Thomas B. Faure, Karen D. Badger, Louis M. Kindt, IBM Corp. (United States); Yutaka Kodera, Toru Komizo, Shinpei Kondo, Takashi Mizoguchi, Satoru Nemoto, Taiiku Saito, Toppan Electronics, Inc. (United States); Richard E. Wistrom, Amy E. Zwebner, IBM Corp. (United States); Kazuhiro Nishikawa, Yukio Inazuki, Hiroki Yoshikawa, Shin-Etsu Chemical Co., Ltd. (Japan). [7823-16]
5:10 pm: Lithography with the advanced binary film photomask. Hiromitsu Mashita, Yingkang Zhang, Takafumi Taguchi, Toshiya Kotari, Shoji Mimotogi, Hiderumi Mukai, Yasushi Itô, Koji Murano, Shinya Yamaguchi, Keiko Morishita, Takashi Hirano, Tomotaka Higaki, Osamu Ikenaga, Hidehiro Watanabe, Toshiba Corp. (Japan). [7823-20]
5:50 pm: Aging study in advanced photomasks: impact of EFM effects on lithographic performance with MoSi binary and attenuated PSM 8% masks. Isabelle Servin, Jérôme Belledent, Marc-Olivier Fialaye, Lab. d’Électronique de Technologie de l’Information (France); Brid Connolly, Matt J. Lamantia, Toppan Photomasks, Inc. (Germany); Karine Julien, Bertrand Le-Griot, STMicroelectronics (France); Laurent Pain, Lab. d’Électronique de Technologie de l’Information (France). [7823-22]

SESSION 6
Room: Ferrante ................. Tues. 1:20 to 2:20 pm
Mask Data Preparation
1:20 pm: Writing 32-nm hp contacts with curvilinear assist features. Aki Fujimura, D2S, Inc. (United States); Byung-Gook Kim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); David H. Kim, Luiminescent Technologies, Inc. (United States); Ingo Bork, D2S, Inc. (United States); Christophe Pierrat, IC Images Technologies Inc. (United States). [7823-26]
2:00 pm: Generalization of shot definition for variable shaped e-beam machines for write-time reduction. Emile Sahouria, Mentor Graphics Corp. (United States); Amanda Bowhill, Mentor Graphics (United States). [7823-118]

SESSION 7
Room: Ferrante ................. Tues. 2:20 to 4:10 pm
Simulation
2:20 pm: Physical resist model calibration for implant level using laser masks. Dongbing Shao, Todd C. Bailey, Mohamed Taib, IBM Corp. (United States); Sajan R. Marakkey, Infinion Technologies North America Corp. (United States). [7823-28]
2:40 pm: Compensation methods using a new single-layer model for buried defects in extreme-ultraviolet lithography masks. Chris H. Clifford, Tina T. Chan, Andrew R. Neureuther, Univ. of California, Berkeley (United States). [7823-29]
3:00 pm: Coffee Break ............. [7823-14]
3:50 pm: An advanced modeling approach for mask and wafer process simulation. Ahmet Karakas, Gau, Inc. (United States). [7823-31]

SESSION 8
Room: Ferrante ................. Tues. 4:10 to 6:30 pm
Optical Proximity Correction
4:10 pm: Attaining the 11-nm node using nonlinear 193-nm exposure addition of interference lithography generated pattern and projection lithography produced line-break patterns that are optimized through source-mask optimization. John S. Petersen, Periodic Structures, Inc. (United States); Ihami Torungohu, Ahmet Karakas, Gau, Inc. (United States). [7823-32]
4:30 pm: Model-based double-dipole lithography for sub-30-nm node device. A-Yoong, Soo Han Choi, Jeong Hoon Lee, SAMSUNG Electronics Ltd. (Korea, Republic of); Ji Young Lee, Mentor Korea Co., Ltd. (Korea, Republic of); James C. Word, Mentor Graphics Corp. (United States). [7823-33]
4:50 pm: SMO mask requirements for low-k lithography. Seiji Nagahara, Kazuaki Yoshimochi, Hiroshi Yamazaki, Akihiko Ando, Takayuki Uchiyama, Ken Nakajima, Renesas Electronics Corp. (Japan). [7823-34]
5:10 pm: Improving model prediction accuracy for ILLT with aggressive SRAFs. Sunggun Jung, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Xin Zh, Luminescent Technologies, Inc. (United States); Woojo Sim, Moon-Gyu Jeong, Jung-Hoon Seo, Sungsoo Suh, Seoung-woon Choi, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Lan Luan, Thomas Cecil, Dong-Hwan Son, Guangming Xiao, David H. Kim, Ki-Ho Baik, Bob Glasgow, Luminescent Technologies, Inc. (United States). [7823-35]
5:30 pm: A systematic study of source-error influence on source-mask optimization. Clovis Alieaume, Emek Yeskala, Vincent Fays, STMicroelectronics (France); Laurent Depre, Vincent Arnaux, Zhipan Li, Brion Technologies, Inc. (United States); Yorick Trouiller, Lab. d’Electronique de Technologie de l’Information (France). [7823-36]
5:50 pm: Impact of model-based fracturing on proximity effect correction methodology. Christophe Pierrat, IC Images Technologies, Inc. (United States); Ingo Bork, D2S, Inc. (United States). [7823-37]
6:10 pm: Fast pixel-based OPC algorithm based on nonparametric kernel regression. Xu Ma, Shiangjiang Jiang, Avideh Zahor, Univ. of California, Berkeley (United States). [7823-38]
Mask Blanks
High-performance photomask technology with the advanced binary film, Koji Murano, Kosuke Taka, Kunihiro Ujigai, Machiko Suenaga, Takeharu Motokawa, Masato Sato, Takahiro Hid tsunami, Osamu Hase, Toshiba Corp. (Japan).

Clean
Advanced photomask cleaning for 32 nm and beyond, Jong-Min Kim, Young-Jin An, Hyo-Jin Ahn, Dong-Seok Lee, Sang-Soo Choi, PKL Co., Ltd. (Korea, Republic of).

Fundamentals and applications of dry CO2 cryogenic aerosol for photomask cleaning, Ivin Varghese, Mehdi Balouch, Charles W. Bowers, Eco-Snow Systems, Inc. (United States).

Program 7823-150
Study on ozonated DI water (DI03) cleaning condition for organic contaminant removal with reduced surface damage to EUV Ru-capping layer, S. Lee, B. Kang, H. Kim, M. Kim, Hanyang Univ. (Korea, Republic of); H. Cho, C. Jeon, H. Ko, H. Lee, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); J. Ahn, J. Park, Hanyang Univ. (Korea, Republic of).

EUV

Process mask correction (MPC) modeling and its application to EUV mask for electron-beam mask writer EBM-7000, Takashi Kamikubo, Takayuki Ohnishi, Shigeiyo Fujita, Hiromi Ogi, Yoshimi Hattori, Shuichi Tashima, NuFlare Technology, Inc. (Japan); Yasuko Saito, Tadahiro Takagawa, Brion Technologies KK (Japan); Shufeng Bai, Jien-Shiang Wang, Rafael C. Howell, George Chen, Jiangwei Li, Jun Tao, James N. Wiley, Brion Technologies, Inc. (United States).

Sensitivity results from a 193-nm EUV-mask inspector, Gregg A. Inderhees, Daniel C. Wack, Tao-Yi Fu, Qiang Zhang, Yalin Xiong, KLA-Tencor Corp. (United States).

Haze
Study on storage components and application performance for haze prevention, Shu Li Chen, Tian-Yang Fang, Ryan Lai, Der Chen Lee, United Microelectronics Corp. (Taiwan).

Inspection
An analysis of correlation between scanning direction and defect detection at ultra-high resolution, Kwon Lim, Sung Pii Choi, Wonil Cho, Dong-Hoon Chung, Chan-Uk Jeon, HanKu Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of).

Feasibility study of EUV patterned mask inspection for the 22-nm node, Dana Bernstein, Applied Materials (Israel); Dong-Hoon Chung, SAMSUNG Electronics Co., Ltd. (Korea, Republic of).

Free form micro-lens arrays enable innovations and more efficiency for mask inspection tools, Ansgar Teipel, Tanja Bizjak, Manfred Jarczynski, Günter Hess, Lutz Aschke, LIMO Lissotschenko Mikrooptik GmbH (Germany).


28N foundry reticle requalification and solutions for IC fabs, Bryan W. Reese, KLA-Tencor Corp. (United States); David Wu, KLA-Tencor Taiwan (Taiwan); Bo Mu, KLA-Tencor Corp. (United States).

Study of EUV-mask inspection technique using DUV-light source for hp-22-nm and beyond, Ryoshi Hiroto, Nobutaka Kikui, Masatoshi Hirono, Advanced Mask Inspection Technology, Inc. (Japan); Kenichi Takahara, Hideaki Hashimoto, NuFlare Technology, Inc. (Japan); Hiroaki Shimamura, Semiconductor Leading Edge Technologies, Inc. (Japan).

Data Preparation
Efficient MDP automation system linkage and verification focusing on Boolean layer generation, George Shiau, United Microelectronics Corp. (Taiwan).

MDP arrangement with mask suppliers for rising OASIS tape out, Erwin Dang, Rachel Lee, United Microelectronics Corp. (Taiwan).

Study of data I/O performance on distributed disk system in mask data preparation, Shuichi Ohara, Nippon Control System Corp. (Japan); Hiroyuki Kodaira, Tomoyuki Chikagawa, Masakazu Hamaj, Yasuharu Yoshioka, Nippon Control System Corp. (Japan).

Proximity effect correction concerning forward scattering, Dai Tsunoda, Nippon Control System Corp. (Japan).

An optimized OPC and MDP flow for reducing mask write time and mask cost, Eillyn Yang, Cheng-Hs Li, Semiconductor Manufacturing International Corp. (China); Yu Zhu, Mentor Graphics Shanghai Electronic Technology Co. (China); Eric G. Guo, Semiconductor Manufacturing International Corp. (China).

Metrology
Ellipsometric investigation of mechanically polished silt and quartz glass, Oleksandr Shestopal, National Taras Shevchenko Univ. of Kyiv (Ukraine).

Thin film metrology by FFT using SE and SR signal, Jangik Park, Yusin Yang, SAMSUNG Electronics Co., Ltd. (Korea, Republic of).


Optimized reticle alignment structures for minimizing aberration sensitivities and pattern shifts, Mark A. van de Kerkhof, Barry Moest, Haico Kok, ASML Netherlands B.V. (Netherlands).

NIL
Duplicated template for discrete track media, Atsushi Tatsugawa, Noriko Yamashita, Tadashi Oomatsu, Kenji Saitou, Takashii Kato, Toshihide Ishikawa, Kazuyuki Usuki, FUJIFILM Corp. (Japan).

Optical Proximity Correction
Optimize the OPC control recipe with cost function, Qingwei Liu, Semiconductor Manufacturing International Corp. (China); Liguo Zhang, Mentor Graphics Shanghai Electronic Technology Co. (China).

OPC recipe optimization using simulated annealing, Tamer S. Desouky, Mentor Graphics Egypt (Egypt).

Qualification methodology of SRAF insertion at contact holes patterning lithography process, Juhwan Kim, Pat J. Lacour, Mentor Graphics Corp. (United States).

CAD for positive line-by-fill SAPD process, Qiao Li, Mentor Graphics Corp. (United States).

A full-chip MB-SRAF placement for advanced technology nodes using the SRAF guidance map, Yin-Wen Lu, Brion Technologies, Inc. (United States); Shigeki Nomia, Masahiro Miyairi, Toshiba Materials Co., Ltd. (Japan); Tatsuo Nishibe, Brion Technologies KK (Japan); Been-Der Chen, Hanying Feng, William Wong, Zhang Wang, Chun Zhu, Min-Chun Tsai, Brion Technologies, Inc. (United States).

Optical proximity correction challenges with highly elliptical contacts, Cristopher M. Cork, Synopsys SARL (France); Levi D. Barnes, Yong Ping, Xiaohai Li, Stephen Jang, Synopsys, Inc. (United States).

Manufacturing cost reduction and extending scanner life by using inverse lithography technology with assist feature, Sung-Ho Jun, Yeon-Ah Shim, Jaeyoung Choi, Kwangsun Choi Jv, Jae-won Han, Dongbu HiTek Co., Ltd. (Korea, Republic of); K-Ho Baik, David H. Kim, Dong-Hwan Son, Xin Zhou, Youngtak Woo, Luminescent Technologies, Inc. (United States).

Aftordable and process window increasing novel mask-writing technique, David H. Kim, Luminescent Technologies, Inc. (United States); Shuichiro Ohara, Nippon Control System Corp. (Japan).

Substrate aware OPC rules for block levels generated using physical resist simulation, Dongbing Shao, Todd C. Bailey, Mohammed Talibi, IBM Corp. (United States).

Multiple models versus single compromise model for doped-poly, double-poly, metal 1 to 3, J. Lawrence, J. Lin, Jianlian Shu, Synopsys, Inc. (United States); Ezequiel Vidal-Russell, Micron Technology, Inc. (United States).

High-pattern density inverse mask design incorporating an innovative image-contrast optimization algorithm, Jue-Chin Yu, Peichun Yu, National Chiao Tung Univ. (Taiwan).

Simultaneous source-mask optimization: a numerical combining method, Thomas Mülders, Synopsys GmbH (Germany); Vitaly M. Domnenko, Synopsys, Inc. (Russian Federation); Bernd Küchler, Thomas Mülders, Synopsys GmbH (Germany); Amyn A. Poowana, Kunal N. Taradave, William A. Stanton, Synopsys, Inc. (United States).

Optimization of double patterning split by analyzing the diffraction orders in the pupil plane, Nasimma Ziegagou, Vincent Fray, Yorick Trouiller, Emek Yesiada, Frederic Robert, STMicroelectronics (France).

Patterning
The CD uniformity improvement for AF/extension using mask DFM (design for manufacturing), Byung-Ho M. Nam, YoungMo Lee, Sunghyun Oh, YongDae Kim, MuriS Kim, Changseon Choi, Tae-Joong Ha, Chang-Reol Kim, Hyung Shin, Mentor Graphics Corp. (Korea, Republic of).

EUV-modified defect mitigation through pattern placement, Mansoor Abbas, John M. Burns, Synopsys, Inc. (United States); Yan A. Liu, Pei-Yang Yan, Intel Corp. (United States).

Integrated mask and optics simulations for corner rounding effect in OPC modeling, Jing Xue, Zhilei Hou, Synopsys, Inc. (United States); Guo Ping, Synopsys Korea Inc. (Korea, Republic of); Yunjiang Zhang, Yongfa Fan, James P. Shiel, Synopsys, Inc. (United States); Thomas Schmoecker, Synopsys GmbH (Germany); Sooyong Lee, Synopsys Korea Inc. (Korea, Republic of).

Wednesday 15 September

Special Session on EBDW/ML2: Opening Remarks and Introductions

Room: Steinbeck Forum .......................... Wed. 8:00 to 10:00 am

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“13.5 nanometer or 17.3 picometer? - we did not drink the Kool-Aid!
From ‘Plenty, but never enough’ to ‘badly needed’ -
are we funding the right technology??”

SESSION 9A
Room: Steinbeck Forum ................. Wed. 8:00 to 10:00 am

Overview Session

8:00 am: Design for e-beam: design insights for direct-write maskless lithography (Invited Paper), Aki Fujimura, DZS, Inc. (United States) .......[7823-127]
8:40 am: Historical Overview, Hans C. Pfeiffer, HCP Consulting Services United States .................................................................[7823-124]
9:00 am: Datapath/Platform/SLM, Tor Sandstrom, Micronic Laser Systems AB (Sweden) .................................................................[7823-125]
9:20 am: Cost/benefit assessment of maskless lithography, C. N. Berglund, Northwest Technology Group (United States) ...................[7823-126]
9:40 am: ML2 in SMT, Stefan Wurm, SEMATECH North (United States) .................................................................[7823-151]

Coffee Break .................................................. 10:00 to 10:30 am

SESSION 9B
Room: Steinbeck Forum .......... Wed. 10:30 to 11:30 am

Use Models and Special Applications Needed

10:30 am: ML2 versus EUV, Shy-Jay Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) .................................................................[7823-123]
10:50 am: Pattern verification for the sub-20-nm era, Ido Holcman, Applied Materials (Israel) .................................................................[7823-128]
11:10 am: EBDW as complementary lithography, David K. Lam, Multibeam Systems Inc. (United States) .................................................................[7823-129]

Open Discussion with Audience Participation
Room: Steinbeck Forum .. Wed. 11:30 am to 12:10 pm

Lunch Break .................................................. 12:10 to 1:20 pm

SESSION 9C
Room: Steinbeck Forum .......... Wed. 1:20 to 2:40 pm

Use Models and Special Applications Needed II

1:20 pm: TBD, ..................................................[7823-130]
1:40 pm: Geometrically induced dose correction method for e-beam lithography applications, Reinhard R. Galler, EQUIcon Software GmbH Jena (Germany); Kang-Hoon Choi, Manuela S. Gutsch, Christoph K. Kohle, Fraunhofer-Ctr. Nanoelektronische Technologien (Germany); Michael Krueger, EQUIcon Software GmbH Jena (Germany); Luis Ramos, Vistec Electron Beam GmbH (Germany); Martin Suelzle, EQUIcon Software GmbH Jena (Germany); Ulf Weidennuebler, Vistec Electron Beam GmbH (Germany) ...........[7823-131]
2:00 pm: Data path challenges, Laurent Pain, Lab. d’Electronique de Technologie de l’Information (France) ..................................................[7823-132]
2:20 pm: TBD, ..................................................[7823-134]

SESSION 10
Room: Ferrante ................. Wed. 1:00 to 3:00 pm

EUV I
Session Chairs: Rik M. Jonckheere, IMEC (Belgium); Frank E. Abboud, Intel Corp.

1:00 pm: A lifetime study of EUV masks, Emily E. Gallagher, Uzodinma Okoroanyanwu, Obert R. Wood II, Louis M. Kindt, Monica J. Barrett, IBM Corp. (United States); Hirokazu Kato, Toshiba America Electronic Components, Inc. (United States); Guillaume Landie, STMicroelectronics (United States) .......[7823-39]
1:20 pm: The control of EUV-mask defects on mask making process, Kuan-Wen Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) .......[7823-40]
1:40 pm: Impact of mask topography and multilayer stack on high-NA imaging of EUV masks, Johannes Ruoff, Carl Zeiss SMT AG (Germany) .......[7823-41]
2:00 pm: EUV-mask stack optimization for enhanced-imaging performance, Eelco Van Setten, ASM-L, Netherlands B.V. (Netherlands); Mircea V. Dusa, ASM Belgium N.V. (Belgium); Robert de Kruif, Natalia Davydova, Kornelis Feenstra, Christian Wagner, ASML Netherlands B.V. (Netherlands); Petra Spies, Tristan Bret, Markus Walbingher, Carl Zeiss SMS GmbH (Germany) .......[7823-42]
2:20 pm: Assessing pattern inspection solutions for EUVL reticles at the 11-nm logic node, Ted Liang, John F. Magana, Firoz A. Ghadiali, Guijing Zhang, Intel Corp. (United States) .................................................................[7823-43]
2:40 pm: EUV-mask inspection technologies for contact (hole) layers for 2-nm hp and beyond, Gregg A. Inderhees, Daniel C. Wack, Tao-Yi Fu, Qiang Zhang, Yalin Xiong, KLA-Tencor Corp. (United States) ...........[7823-44]

Coffee Break .................................................. 3:00 to 3:30 pm

Sessions 9C,9D runs concurrently with sessions 10,11.
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<td>Sessions 9C, 9D runs concurrently with sessions 10, 11.</td>
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<tr>
<td>2:40 pm:</td>
<td>Cell projection use in maskless lithography for sub-32-nm logic nodes, Akio Yamada, Advantest Corp. (Japan)</td>
<td>[7823-137]</td>
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<tr>
<td>3:00 pm:</td>
<td>REBL: reflective electron-beam lithography for high-throughput direct-write patterning, Mark A. McCord, Paul Petric, Chris Bevis, Alan Carroll, Alan D. Brodie, Upen德拉 Ummenthaler, Luca Grella, Regina G. Freed, KLA-Tencor Corp. (United States)</td>
<td>[7823-138]</td>
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<tr>
<td>3:50 pm:</td>
<td>Multishaped-beam (MSB): an evolutionary approach for high-throughput e-beam lithography, Matthias Stolowski, Hans-Joachim Doring, Ines A. Stolberg, Wolfgang H. Dori, Vistec Electron Beam GmbH (Germany)</td>
<td>[7823-139]</td>
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<tr>
<td>4:10 pm:</td>
<td>High-throughput maskless lithography, Bert J. Kamperberke, MAPPER Lithography (Netherlands)</td>
<td>[7823-140]</td>
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<tr>
<td><strong>SESSION 11</strong></td>
<td>Room: Ferrante</td>
<td>Wednesday, 3:30 to 5:30 pm</td>
<td>EUV II</td>
<td>Session Chairs: HanKu Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Paul W. Ackmann, GLOBALFOUNDRIES Inc.</td>
</tr>
<tr>
<td>3:30 pm:</td>
<td>Investigation of carbon contamination growth dependency on Ruthenium surface property of EUV mask, Han-Shin Lee, Jae-Hyuck Choi, DongGun Lee, DaeHyuck Kang, Hyungho Ko, SeongSu Kim, Chan-Uk Jeon, HanKu Cho, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)</td>
<td>[7823-45]</td>
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<tr>
<td>3:50 pm:</td>
<td>Current status and challenges in EUV reticle defect detection: a case study of using a real product, John F. Magana, Manish Chandhok, Timothy F. Crimmins, Firoz A. Ghadiali, Ted Liang, Guojing Zhang, Intel Corp. (United States)</td>
<td>[7823-46]</td>
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<tr>
<td>4:10 pm:</td>
<td>Natural EUV-mask blank defects: evidence, timely detection, analysis, and outlook, Dieter Van den Heuvel, Rik M. Jonckheere, Eric Hendrickx, Shaunee Y. Cheng, Kurt G. Ronse, IMEC (Belgium)</td>
<td>[7823-47]</td>
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<tr>
<td>4:30 pm:</td>
<td>Printability of EUVL mask defect detected by actinic blanks inspection tool and 199-nm pattern inspection tool, Takashi Kamo, Tsuneo Terasawa, Takeshi Yamane, Hiroyuki Shimamura, Noriaki Takagi, Tsuyoshi Amano, Toshitomo Tanaka, Kazuo Tawarayama, Osamu Suga, Ichiro Morii, Semiconductor Leading Edge Technologies, Inc. (Japan)</td>
<td>[7823-48]</td>
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<tr>
<td>4:50 pm:</td>
<td>Improvement of actinic blank inspection and phase defect analysis, Takashi Yamane, Toshitomo Tanaka, Tsuneo Terasawa, Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan); Tom K. Castro, Numonyx California Technology Ctr. (United States); Brid Connolly, Toppan Photomasks, Inc. (Germany)</td>
<td>[7823-49]</td>
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<tr>
<td>5:10 pm:</td>
<td>Investigation of the influence of resist patterning on absorber LWR for 22-nm-node EUV lithography, Yuichi Inazuki, Tsukasa Abe, Taichi Ogase, Satoshi Kawashima, Tadahiko Takigawa, Hiroshi Mohri, Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)</td>
<td>[7823-142]</td>
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**Thursday 16 September**

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<th>Chairs</th>
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<tr>
<td><strong>SESSION 12</strong></td>
<td>Room: Steinbeck Forum</td>
<td>Thurs., 8:00 to 9:00 am</td>
<td>Mask Business</td>
<td>Session Chairs: Bryan S. Kasprzowicz, Photronics, Inc.; Artur P. Balasinski, Cypress Semiconductor Corp.</td>
</tr>
<tr>
<td>8:00 am:</td>
<td>Mask shop automation: station controllers for photomask manufacturing, Venkatesh Nadamuni, Derek Lager, Intel Corp. (United States)</td>
<td>[7823-50]</td>
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<td>9:00 am:</td>
<td>Defect reduction through lean methodology, Kathleen Purdy, Louis M. Kindt, Jim Densmore, Craig Benson, Nancy C. Zhou, John Leonard, Cynthia Whiteside, Robert Nolan, David E. Shanks, IBM Corp. (United States)</td>
<td>[7823-51]</td>
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<tr>
<td>9:40 am:</td>
<td>How to match without copying: an approach for APSM mask process matching using aerial imaging, Martin Sczyba, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Carmelo Romeo, Numonyx Agrate (Italy); Frank Schurack, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Tom K. Castro, Numonyx California Technology Ctr. (United States); Brid Connolly, Toppan Photomasks, Inc. (Germany)</td>
<td>[7823-52]</td>
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**SESSIONS 13, 14, 15 run concurrently with sessions 17, 18, 19.**

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<tr>
<td><strong>SESSION 13</strong></td>
<td>Room: Steinbeck Forum</td>
<td>Thurs., 9:00 to 10:20 am</td>
<td>Mask Repair</td>
<td>Session Chairs: Ronald R. Bozak, RAVE LLC; Peter D. Buck, Toppan Photomasks, Inc.</td>
</tr>
<tr>
<td>9:00 am:</td>
<td>Advanced laser mask repair in the current wafer foundry environment, Todd E. Robinson, RAVE LLC (United States)</td>
<td>[7823-53]</td>
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<tr>
<td>9:20 am:</td>
<td>Impact of new MoSi mask compositions on processing and repair, Anthony D. Garetto, Carl Zeiss SMT Inc. (United States); John B. Stuckey, Donald H. Butler, MP Mask Technology Ctr., LLC (United States)</td>
<td>[7823-54]</td>
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<tr>
<td>9:40 am:</td>
<td>Prospect of EUV mask repair technology using e-beam tool, Shingo Kanamitsu, Takashi Hirano, Toshiba Corp. (Japan); Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan)</td>
<td>[7823-55]</td>
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<tr>
<td>10:00 am:</td>
<td>Study of EUV mask defect repair using FIB method, Tsuyoshi Amano, Hiroyuki Shimamura, Noriaki Takagi, Tsunee Terasawa, Osamu Suga, Semiconductor Leading Edge Technologies, Inc. (Japan); Kensei Shinya, Fujio Aramaki, Anto Yasaka, SiNanoTechnology Inc. (Japan); Yuichi Inazuki, Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)</td>
<td>[7823-56]</td>
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<td>10:20 am:</td>
<td>Coffee Break:</td>
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<tr>
<td><strong>SESSION 17</strong></td>
<td>Room: Ferrante</td>
<td>Thurs., 9:00 to 11:10 am</td>
<td>Metrology I</td>
<td>Session Chairs: John M. Whitley, KLA-Tencor Corp.; David Y. Chan, SEMATECH North</td>
</tr>
<tr>
<td>9:00 am:</td>
<td>Detecting measurement outliers: reevaluate efficiently, Albrecht Ulrich, Advanced Mask Technology Ctr. GmbH Co. KG (Germany)</td>
<td>[7823-72]</td>
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<tr>
<td>9:20 am:</td>
<td>Advanced mask CD MTT correction technique through improvement of CD measurement repeatability of CD SEM, Chooqhanh Ryu, Hoyong Jung, Tae-Joong Ha, Chang-Reol Kim, Hynix Semiconductor Inc. (Korea, Republic of)</td>
<td>[7823-73]</td>
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<tr>
<td>9:40 am:</td>
<td>Improving registration measurement capability by defining a 2D grid standard using multiple registration measurement tools, Oliver Löfler, Albrecht Ulrich, Gunter Antesberger, Jan Richter, Andreas Wiswesser, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Masaru Iyuzuki, Tatsuhiko Kamibayashi, Toppan Printing Co., Ltd. (Japan); Frank Laske, Dieter K. Adam, Michael Ferber, Klaus-Dieter Roeth, KLA-Tencor MIE GmbH (Germany)</td>
<td>[7823-74]</td>
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<tr>
<td>10:00 am:</td>
<td>CD-signature determination by Nurfle inspection tool, Jan Richter, Jan P. Heumann, Christian U. Utzny, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Noriyuki Takamatsu, Shuichi Tamamushi, NuFlare Technology, Inc. (Japan)</td>
<td>[7823-75]</td>
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<td>10:20 am:</td>
<td>Coffee Break:</td>
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Thursday 16 September (continued)  
Sessions 13-14-15 run concurrently with session 17-18-19.

SESSION 14
Room: Steinbeck Forum ........... Thurs. 10:50 am to 12:30 pm
Mask Cleaning
Session Chairs: Michael D. Archuleta, RAVE LLC; Anna Tchikoulaeva, GLOBALFINDRIES Inc. (Germany)
10:50 am: Study and improvement approach to 193-nm radiation damage of attenuated phase-shift mask, Tomohito Hirose, Hitomi Tsukuda, Yosuke Kojima, Hayato Ida, Takashi Haraguchi, Tsyoshi Tanaka, Toppan Printing Co., Ltd. (Japan) .................................................. [7823-57]
11:10 am: Fundamental study of droplet spray characteristics in photomask cleaning for advanced lithography, Chi-Lun Wei, Hung Liu, Ting Hao Hsu, Sheng-Chi J. Chin, Shin Chang Lee, Anthony Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Gaston Lee, Shunho Yang, HamaTech APE GmbH & Co. KG (Taiwan); Peter Dress, HamaTech APE GmbH & Co. KG (Germany); Sherjag Singh, Uwe Dietze, Hamatech USA, Inc. (United States) .................. [7823-68]
11:30 am: Qualification of BitClean™ technology in photomask production, Tod E. Robinson, RAVE LLC (United States) .................. [7823-59]
11:50 am: Confirmation about degradation of capping layer in some kinds of cleaning condition, Noriaki Takagi, Semiconductor Leading Edge Technologies, Inc. (Japan)
12:10 pm: Study of the airborne SO₂ and NH₃ contamination on Cr, MoSi, and quartz surfaces of photomasks, Herve Fontaine, Virginie Enyedi, Sylviane Cotre, Lab. d’Electroménent de Technologie de l’Information (France) .................. [7823-61]
Lunch Break ........................ [12:30 to 1:50 pm]

SESSION 15
Room: Steinbeck Forum ........... Thurs. 1:50 to 3:10 pm
Inspection I
Session Chairs: William H. Broadbent, KLA-Tencor Corp.; Emily E. Gallagher, IBM Corp.
1:50 pm: Electron-beam inspection of NGL reticles, Sterling Watson, David S. Alles, Gregg A. Inderhees, KLA-Tencor Corp. (United States) .................. [7823-62]
2:10 pm: EUV-mask defecisty study by existing DUV tools and new e-beam technology, Ilan Englard, Applied Materials BV (Netherlands); Rik M. Jonckheere, Dieter Van Den Heuvel, IMEC (Belgium); Shmoolik Mangan, Amiad Conley, Moshe Rozentsvige, Doron Meshulach, Applied Materials (Israel); Robert Schreutelkamp, Gaetano Santoro, Applied Materials (Belgium); Vladislav Kudrina, Sheng-Chi J. Chin, Shin Chang Lee, Anthony Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Fei Wang, Long E. Ma, Yan Zhao, Chiyuan Kuan, Hong Xiao, Jack Y. Jau, Hermes-Microvision Inc., USA (United States) .................. [7823-64]
2:30 pm: Native pattern defect inspection on 88-nm HP dense pattern using advanced electron-beam inspection system, Takeya Shimomura, Dai Nippon Printing Co. America, Inc. (United States); Yuichi Inazuki, Tokuasa Abe, Tadahiko Takikawa, Hiroshi Mohri, Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan); Fei Wang, Long E. Ma, Yan Zhao, Chiyuan Kuan, Hong Xiao, Jack Y. Jau, Hermes-Microvision Inc., USA (United States) .................. [7823-64]
2:50 pm: Development of EB inspection system(EBeyeM) for EUV mask, Takashi Hirano, Shinji Yamaguchi, Masato Nakai, Masanitu Tto, Yuzuhiko Yamazaki, Motoki Kadowaki, Tooru Kikole, Toshiba Corp. (Japan); Norio Kimura, Hiroshi Sobukawa, Kenji Terao, Masahiro Hatakeyama, Takeshi Murakami, Kiyam Suakarno, Takehide Hayashi, Chiyan Kuan, Hong Xiao, Jack Y. Jau, Hermes-Microvision Inc., USA (United States) .................. [7823-65]
3:10 pm: Coffee Break

SESSION 16
Room: Steinbeck Forum ........... Thurs. 3:40 to 5:20 pm
Inspection II
Session Chairs: James E. Potzick, National Institute of Standards and Technology; Larry S. Zurbrick, Agilent Technologies, Inc.
3:40 pm: Study of shape evaluation for mask and silicon using large field of view, Ryoshi Matsuka, Hitachi High-Technologies Corp. (Japan) .................. [7823-66]
4:00 pm: New strategies for mask noise reduction, Aviram Tam, Yulian Wolff, Michael Ben-Yishai, Shmoolik Mangan, Applied Materials (Israel) .................. [7823-67]
4:20 pm: Inspection of advanced computational lithography logic reticles using a 193-nm inspection system, Ching-Fang Yu, Mei-Chun Lin, Mei-Tsu Lai, Luke T. H. Hsu, Angus Chin, S. C. Lee, Anthony Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Jim Wang, Ellison Chen, David Wu, KLA-Tencor Taiwan (Taiwan); William Broadbent, William Huang, Jinggang Zhu, KLA-Tencor Corp. (United States) .................. [7823-68]
4:40 pm: Lithographic pattern recovery (LPR) for sub-32-nm mask defect review and classification, Vikram L. Tolani, Thuc Dinh, Danping Peng, Lin He, Linyong Pang, Luminence Technologies Inc., USA (United States); Tatsuya Sato, Tatsuya Sato, Toppan Printing Co., Ltd. (Japan) .................. [7823-70]
5:00 pm: Computational lithography and inspection (CLI), and its applications in mask inspection, metrology, review, and repair, Linyong Pang, Danping Peng, Dongqun Chen, Lin He, Vikram L. Tolani, Luminence Technologies Inc., USA (United States) .................. [7823-71]
Attend an SPIE Course

Photomask Fabrication and Technology Basics
SC579
(Duff), Monday 8:30 am to 5:30 pm, $540 / $640

Electron Beam Inspection - Principles and Applications in IC and Mask Manufacturing
SC1009 NEW
(Xiao), Monday 1:30 to 5:30 pm, $335 / $385

Electron Beam Lithography using Massively Parallel Pixel Projection
SC991 NEW
(Pfeiffer), Monday 8:30 am to 12:30 pm, $335 / $385

EUV Lithography
SC888 NEW
(Bakshi), Monday 8:30 am to 5:30 pm, $755 / $855

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- International Centre for Theoretical Physics (ICTP) Winter College
- Visiting Lecturers Program

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This profile combined with the responses to past surveys represents both the business and technical status of the critical mask industry.

A multitude of questions result in a detailed profile of mechanisms, delivery times, returns, and services. Within each category is a series of questions that result in a detailed profile of the technical and business status of the mask industry as an objective assessment of its overall condition. The survey is designed with the input of semiconductor company mask technologists and merchant mask suppliers. This year's assessment is the eighth in the current series of annual reports. With ongoing industry support, the report can be used as a baseline to gain perspective on the technical and business status of the mask and microelectronics industries. It will continue to serve as a valuable reference to identify the strengths and opportunities of the mask industry. The results will be used to guide future investments pertaining to critical path issues. This year's survey is basically the same as the 2005 through 2009 surveys. Questions are grouped into categories: General Business Profile Information, Data Processing, Yields and Yield Loss Mechanisms, Delivery Times, Returns, and Services. Within each category is a multitude of questions that result in a detailed profile of both the business and technical status of the critical mask industry. This profile combined with the responses to past surveys represents a comprehensive view of changes in the industry.

**EUV lithography has been highlighted for the lithography technique development based on proven multibeam projection technology**

E. Platzgummer, S. Cernusca, P. Joechl, C. Klein, S. Kvasnica, H. Loeschner, IMS Nanofabrication AG (Austria)

**conclusions**

We have achieved the best performance in etching the two-layered EUV absorber and in small CD shift for EUV masks in 22nm generation and beyond. The results obtained by a series of our experiments indicate that the deposition of by-product to sidewall during absorber etching, which we can control by plasma density and vacuum exhaustion during etching process step plays an important role for controlling etch profile and minimizing CD shift.

**Improvement of mask write time for curvilinear assist features at 22 nm**

A. Fujimura, I. Bork, D2S, Inc. (United States); T. Kiuchi, T. Komagata, Y. Nakagawa, JEOL Ltd. (Japan)

In writing 22nm logic contacts with 193nm immersion, curvilinear sub-resolution assist features will be desirable on masks. Curvilinear sub-resolution assist features are good for high volume chips where the wafer volume outweighs considerations for mask write times. For those chips, even 40 hour write times are tolerated for mask writing. For lower-volume production of SOC designs, such write times are economically unacceptable. 8 to 12 hours of write times are feasible for these designs. Previous papers at 2010 Photomask Japan described design for e-beam (DFEB) techniques using circular apertures on production e-beam writers that reduced e-beam write-times by nearly a factor of two. This put the curvilinear assist features within the realm of high-volume production. However, the write times are still too long for SOC designs. This paper describes a new technique that reduces the write time by another factor of two. Resist-exposed SEM images will be shown, written by a production mask writer. E-beam write time comparisons will be made with the conventional methods, demonstrating the additional factor of two improvement.
Multi-beam writing becomes mandatory for future technology nodes in order to stay within reasonable realization times for leading-edge complex masks and templates. IMS Nanofabrication has developed multi-beam projection techniques implementing a programmable aperture plate system (APS) and charged-particle projection optics with 200x reduction. Proof-of-concept of multi-beam writing on static substrates was demonstrated in 2009 using the CHARPAN tool with ion multi-beams and the RIMANA tool with electron multi-beams [1].

For the first time projection multi-beam writing on moving substrates will be presented as made achievable by upgrading the CHARPAN Tool with a laser-interferometer controlled stage. In Q4 2009 the development of a 50 keV electron multi-beam Mask Exposure Tool (eMET) was started. [2, 3]

The eMET development status will be presented and the possible writing times for leading-edge masks and templates will be discussed.

[3] Elmar Platzgummer et al., PMJ 2010

7823-08, Session 2

Multi-shaped e-beam technology for mask writing

J. Gramss, Vistec Electron Beam GmbH (Germany); M. Sczyrba, T. Wandel, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); H. Doering, Vistec Electron Beam GmbH (Germany); A. Stoeckel, U. Weidenmueller, M. Bloecher, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); M. Finken, D. Melzer, EQUIcon Software GmbH (Germany)

Lithography for the 22nm technology node and beyond requires new approaches in regard to both equipment as well as mask design. Multi Shaped Beam technology (MSB) as one of these approaches has already been presented in several publications [1, 2, 3]. The MSB concept is very effective and evolutionary extension of the well established Variable Shaped Beam (VSB) technique and has been successfully reduced to practice. The productivity gain of MSB over VSB increases with decreasing node dimensions/technology, which makes that concept very attractive for future mask fabrication. The present paper describes in detail the working principles and advantages of the MSB approach for mask write application. In that approach MSB electron-optical column, x/y stage and data path are integrated into a fully operational electron-beam lithography system. The special requirements for a Multi E-beam Mask Writer concerning computational lithography will be discussed and their implementation will be shown. Topics of immediate interest starting with the data preparation of aggressive OPC layouts and covering such important features like achievable shot count reduction, data path architecture, write time simulation and several aspects of the exposure process sequence.

As an example analysis results of both MSB processing- and write time of full 32nm critical layer mask layouts will be presented. In addition, exposure results illustrating the current status of system integration will be given.

Fig.1: Schematic comparison of single variable shaped beam VSB (left) and Multi Shaped Beam MSB (right) technique
Fig.2: Multi Shaped Beam test system


7823-09, Session 2

Multiple-beam mask writers: an industry solution to the write-time crisis

L. C. Litt, G. P. Hughes, SEMATECH North (United States)

The semiconductor industry is under constant pressure to reduce production costs even as technology complexity increases. Lithography represents the most expensive process due to its high capital equipment costs and the implementation of low-k1 lithographic processes, which has added to the complexity of making masks through the growth of optical proximity correction, pixelated masks, and double or triple patterning. Each of these mask technologies allows the production of semiconductors at future nodes while extending the utility of current immersion tools.

Low-k1 patterning complexity combined with increased data due to smaller feature sizes is driving extremely long mask write times. While a majority of the industry is willing to accept mask write times of up to 24 hours, evidence suggests that the write times for many masks at the 22 nm node and beyond will be significantly longer.

It has been estimated that $50M+ in Non Recurring Engineering costs will be required to develop a multiple beam mask writer system, yet the business case to recover this kind of investment is not strong. Moreover, funding such a development is a high risk for an individual supplier. The problem is compounded by a disconnect between the tool customer (the mask supplier) and the final mask customer which will bear the increased costs if a high speed writer is not available. Since no individual company will likely risk entering this market, some type of industry-wide funding model will be needed.

Because SEMATECH’s member companies strongly support a multiple beam technology for mask writers to reduce the write time and cost of 193 nm and EUV masks, SEMATECH plans to pursue an advanced mask writer program in 2011 and 2012. In 2010, efforts will focus on identifying a funding model to address the investment to develop such a technology.

7823-10, Session 2

Resist process windows in electron-beam lithography

A. T. Jamieson, N. Wilcox, W. Y. Kwok, Y. K. Kim, Intel Corp. (United States)

High resolution SRAFs are challenging to pattern, especially on photomasks with pattern density variations & beam corrections. This paper will present analysis techniques of SRAF resist resolution performance and manufacturing robustness. Electron beam proximity effects and their correction methods have substantial impacts on aerial image quality. Resist resolution & LER depend strongly on the aerial image, and these effects will be looked at theoretically and experimentally with top down CD SEM & reflected die-to-die inspection techniques. A quantitative understanding of resolution process latitude is important in SRAF patterning, especially when one considers beam corrections that are used to compensate for effects like electron fogging, etch loading effects, dose maps, etc. The magnitude & nature of these corrections vary substantially, and impact resolution requirements. The analysis techniques presented are helpful in optimizing data / dose bias as well, and this will also be discussed.
Process window improvement on 45-nm technology nonvolatile memory by CD uniformity correction

U. Buttgereit, R. Birkner, Carl Zeiss SMS GmbH (Germany); E. Graitzer, A. Cohen, Carl Zeiss SMS GmbH (Israel); B. Triulzi, C. Romeo, Numonyx Agrate (Italy)

For the next years optical lithography stays at 193nm with a numerical aperture of 1.35. Mask design becomes more complex, mask and lithography specification tighten and process control becomes more important than ever. Accurate process control is a key factor to success to maintain a high yield in chip production.

One of the key parameters necessary to assure a good and reliable functionality of any integrated circuit is the Critical Dimension Uniformity (CDU). There are different contributors which impact the total wafer CDU: mask CD uniformity, scanner repeatability, resist process, lens fingerprint, wafer topography etc.

In this work we focus on improvement of intra-field CDU at wafer level by improving the mask CD signature using a CDC200 tool from Carl Zeiss SMS. The mask layout used is a line and space dark level of a 45nm node Non Volatile Memory (NVM). A prerequisite to improve intra-field CDU at wafer level is to characterize the mask CD signature precisely. For CD measurement on mask the newly developed wafer level CD metrology tool WLCDD32 of Carl Zeiss SMS was used. The WLCDD32 measures CD based on proven aerial imaging technology. The WLCDD32 measurement data show an excellent correlation to wafer CD data. For CDU correction the CDC200 tool is used which utilizes an ultrafast fem-to-second laser to write intra-volume shading elements (Shade-In Elements) inside the bulk material of the mask. By adjusting the density of the shading elements, the light transmission through the mask is locally changed in a manner that improves wafer CDU when the corrected mask is printed.

In the present work we will demonstrate a closed loop process of WLCDD32 and CDC200 to improve mask CD signature as one of the main contributors to intra-field wafer CDU. Furthermore we will show that the process window will be significantly enlarged by improvement of intra-field CDU. An increase of 20% in exposure latitude was observed.

Degradation of pattern quality due to strong electron scattering in EUV mask


Based on simulation and experiment, we present the degradation of pattern quality in EUV photomask. This degradation mainly comes from the strong electron scattering in Mo/Si multi-layer of EUV mask with high atomic number. Here, we discuss the electron distribution of EUV mask compared with conventional optical mask by using Monte-Carlo simulation. Especially, the patterning qualities such as proximity effect and exposure latitude are checked by both experiment and simulation.

According to the specifications of EUV photomask for sub 28nm device, in this paper, we present the requirements of e-beam mask writer and resist, for example, grid size for proximity effect correction in mask writer, resist sensitivity, exposure latitude and so on.

Plasma monitoring of chrome dry etching for mask making

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As mask feature size shrinks, it is required that the improvement of the mask qualities. In a photomask fabrication, Cr dry etching process is one of the most critical steps which define the performance of the critical dimensions (CD). In consequence, plasma condition should be maintained stable in the etch chamber from the point of view of mask-to-mask or chamber-to-chamber matching.

In this work, the methodology using plasma monitoring tools is introduced; optical emission spectroscopy (OES) and self-excited electron resonance spectroscopy (SEERS). After monitoring the plasma state with these tools, plasma condition can be categorized with respect to the signature of the spectrum, the electron collision rate, and the electron density distribution.

At the end, it is possible to predict the CD performance of the time, by checking the specific plasma parameters.

Long-range proximity effects and CD variation: a method to characterize chemical flare and develop loading

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Variations in critical dimension (CD) as a function of the proximity of an individual feature to other exposed areas within the die are a continuing problem in both mask fabrication and optical lithography. For example the linewidth of a given feature next to an array of sparse features can be different than the same feature that is close to an area that received a higher net exposure. These pattern density effects will continue to get worse as feature sizes decrease below 32 nm.

There are believed to be two sources of resist related pattern density effects in chemically amplified photoresists. The first is due to acid volatility, where photogenerated acid is presumed to redeposit on the wafer or mask during exposure or bake; here we refer to this effect as chemical flare. The second is develop loading which refers to the impact of local depletion of developer in highly exposed regions. Develop loading and chemical flare can occur separately or simultaneously and they can cause deviations in feature size that may be difficult to correct for by adjustment of the exposure process.

In this report we describe a technique that allows the effects of chemical flare and develop loading to be separately characterized. The method makes use of patterned arrays of exposure sites consisting of a series of line/space patterns that are either isolated or in proximity to highly exposed pads. The substrates are developed employing a custom liquid flow cell designed to provide a unidirectional laminar flow across the patterned arrays and we can independently measure the effects of chemical flare and develop loading. We will describe results for both negative and positive tone resists under e-beam and DUV exposure.

New method to determine process window considering pattern failure

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In general, available process window in experiment is smaller than that from focus-exposure matrix (FEM) simulation due to pattern failures, such as pattern collapse or pattern bridging. However Available process window is difficult to be expected by verifying
critical dimension (CD) results only. In order to predict pattern failures precisely, additional information is required, such as image log slope (ILS) or resist profile as well as CD information. Since ILS is inversely proportional to line edge roughness (LER), it can be very useful metric to predict pattern failures. However, ILS as calculated from areal image, it does not include resist process effects on pattern fidelity. Also resist profile may have vertical slope even when areal image has low contrast within photo resist.

In this paper, effective acid distribution ILS (AILS) is proposed in order to predict available process window more precisely. Effective acid distribution is calculated with Sentaurus lithography TM by SYNOPSIS. In general, effective acid distribution is varied along z axis. Therefore AILS is calculated at the top and bottom of resist separately.

Two hotspot points found experimentally are verified with simulations. Large amount of LER is observed at the edges crossed by cut line. It is difficult to estimate serious LER from simulated resist profile because stochastic acid distribution is not considered in resist model. Even though some lithography simulator adapts stochastic acid diffusion in resist model but it requires much longer calculation time. However, worse LER is simply predicted based on low contrast of effective acid distribution at the cut line region. Large amount of resist loss is expected with simulated resist profile but it is not shown clearly, which is difficult to be detected from SEM image. Resist top loss can also be predicted by evaluating AILS at top 10%.

With evaluating the combination of AILS’s at top and bottom 10%, pattern fail can be determined more clearly. Therefore process condition and layer design will be optimized through the new powerful method, AILS.

7823-17, Session 3

A systematic approach to the determination of SRAF capabilities in high-end mask manufacturing

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As circuit pattern dimensions continue to shrink, the design of integrated chips becomes very challenging. In combination with a continuous extension of immersion lithography a tremendous increase in use of resolution enhancement techniques (RET) is required. RET on mask level range from heavy use of optical proximity correction (OPC) to the application of sub resolution assist features (SRAFs), e.g. scatter bars. The application of SRAFs is driving mask processes' pattern resolution limits. For 45nm design rules SRAF sizes tended to be much larger than the resolution capability of chemically amplified resists (CARs). However beginning with 32nm and smaller technology nodes, SRAF sizes have decreased to ≤ 80nm which exceeds the resolution limit of some CARs. This results in mask making processes being often incapable of meeting customer requirements. Additionally the complexity of SRAFs in advanced mask data designs require relatively short lengths leading to a more complex, two dimensional problem for mask makers. The SRAF resolution problem is further compounded by complex designs requiring dual tone SRAFs on the same mask (i.e. clear and opaque SRAFs). New CARs and mask processes will have to fulfill all of these SRAF requirements.

When mature 50kV mask processes are extended to meet 32nm design rules and beyond, mask makers encounter small resolved SRAFs with insufficient pattern stability. When inspected at maximum sensitivity, these unstable SRAFs cause nuisance detections which are normally not a concern from a wafer printing point of view. But a very high number of nuisance detections will then overwhelm the number of real mask defects making it impossible to separate the two defect types in a production environment.

To address SRAF resolution gaps with new mask processes or CARs, mask developers must check in detail the capability to resolve SRAFs in a manner that masks pass tight inspections with a low number of nuisance detections. To this end, the AMTC has developed a test mask design and methodology to systematically investigate SRAF resolution and quality for new CARs and new processes. This new design systematically varies SRAF width, length and background pattern density, as well as incorporating non-straight SRAF shapes to cover complex SRAF solutions on customer devices. In addition, the pattern encompasses both tones in order to robustly determine the SRAF resolution capability. The quality assessment of the SRAFs is being done by a tight inspection of the test pattern instead of using cross sectional or top down SEM image review or SEM metrology. This approach inhibits the advantage to use the same mask quality assessment in the development as it is being used in production later on.

In this paper we report upon our findings in applying this new methodology to both mature and new 50kV e-beam CARs as well as to different mask substrates. Results of this new methodology were compared to limitations observed on customer masks in order to judge the effectiveness in predicting SRAF resolution capability on products.

7823-116, Session 3

Reduced basis method for source mask optimization

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Image modeling and simulation are critical to extending the limits of leading edge lithography technologies used for IC making. Simultaneous source mask optimization (SMO) has become an important objective in the field of computational lithography. SMO is considered essential to extending immersion lithography beyond the 45nm node. However, SMO is computationally extremely challenging and time-consuming. The key challenges are due to run time vs. accuracy tradeoffs of the imaging models used for the computational lithography.

We present a new technique to be incorporated in the SMO flow. This new approach is based on the reduced basis method (RBM) applied to the simulation of light transmission through the lithography masks. It provides a rigorous approximation to the exact lithographical problem, based on fully vectorial Maxwell’s equations. Using the reduced basis method, the optimization process is divided into an offline and an online steps. In the offline step, a RBM model with variable geometrical parameters is built self-adaptively. In the online step, the RBM model can be solved very fast for arbitrary illumination and geometrical parameters, such as dimensions of OPC features, line widths, etc. This approach dramatically reduces computational costs of the optimization procedure while providing accuracy superior to the approaches involving simplified mask models. RBM furthermore provides rigorous error estimators, which assure the quality and reliability of the reduced basis solutions.

We apply the reduced basis method to a 3D SMO example. We quantify performance, computational costs and accuracy of our method. We compare the run time and the accuracy tradeoffs involving RBM, EMF and Kirchhoff mask models.

7823-18, Session 4

Development and characterization of a thinner binary mask absorber for 22-nm node and beyond

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The lithography challenges posed by the 22 nm node continue to place stringent requirements on photomasks. The dimensions of the mask features continue to shrink more deeply into the sub-wavelength scale. In this regime residual mask electromagnetic field (EMF) effects due to mask topography can degrade the imaging performance of critical mask patterns by degrading the common lithography process window and by magnifying the impact of mask errors or MEEF. Based on this, an effort to reduce the mask topography effect by decreasing the thickness of the mask absorber was conducted. In this paper, we will describe the results of our effort to develop and characterize a binary mask substrate with an absorber that is approximately 20-25% thinner than the absorber on the current Opaque MoSi on Glass (OMOG) binary mask substrate.

For expediency, the thin absorber development effort focused on using existing absorber materials and deposition methods. It was found that significant changes in film composition and structure were needed to obtain a substantially thinner blank while maintaining an optical density of 3.0 at 193 nm. Consequently, numerous studies to assess the mask making performance of the thinner absorber material were required and will be described. The results of studies of film stress, mask flatness, mask image placement, cleaning durability, dry etching performance, and critical dimension performance will be shown. During these studies several significant mask manufacturing constraints of the thin absorber were discovered. The lower film stress and thickness of the new absorber resulted in improved mask flatness and up to a 60% reduction in process-induced mask pattern placement change. Improved cleaning durability was another benefit. Furthermore, the improved EMF performance of the thinner absorber [1] was found to have the potential to relieve mask manufacturing constraints on minimum opaque assist feature size and opaque corner to corner gap.

In addition to assessing the mask processing characteristics of the thinner absorber, a detailed assessment of the mask defect inspection performance was conducted. Results from both reticle plane and aerial plane inspection testing using programmed defect test masks were acceptable and will be shown.

Based on the results of the numerous mask making studies performed to date, the thinner absorber has been found to be suitable for use for fabricating masks for the 22 nm node and beyond.


7823-19, Session 4

**Advanced binary film for 193-nm lithography extension to sub-32-nm node**

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Use of optical lithography is still continuing as the principle technology beyond the 32nm half-pitch generation. However, one of the issues stated in general is the increase in cost. The proportion of the mask fabrication cost of the total lithography cost depends on the wafer volume and is increasing, particularly for the double patterning generation. To reduce overall mask cost, prolonging the mask lifetime is very effective. The factors shortening the mask lifetime are damage by cleaning and by irradiation of 193nm excimer laser during wafer exposure. In order to solve these issues, a novel absorber was developed that is more durable against 193nm irradiation at wafer exposure, and has higher cleaning durability.

Advanced Binary Film (ABF) for the next generation achieved excellent progress in mask cleaning durability. This opens up a wider choice of process chemistries to optimize cleaning conditions, resulting in an increase in final cleaning yield. Higher mask quality and improved process times are expected. In addition, mask lifetime will be extended, because the degradation of mask characteristics caused by multiple cleaning required for re-pelliclization should be minimized. Recently, it has been reported that absorber films are transformed by 193nm excimer laser irradiation and the lithography performance is reduced. Solving this issue is the primary objective of the ABF development. The ABF realized negligible impact after 193nm irradiation so significant improvements in mask lifetime are expected, especially for issues related to absorber degradation.

As a result, it leads to the reduction of the total lithography cost. The ABF, with an Optical Density of greater than 3 and equivalent optical characteristics to present binary mask absorbers, such as reflectivity, benefits from a thinner film compared to present commercially available films. From the wafer printing point of view reduction of mask topography effects is expected of this film. Furthermore, this film will enable thinner resist utilization to obtain the resolution required for the sub-32 nm node.

In this presentation at the conference, both basic blanks and patterning characteristics required on masks will be reported.

7823-20, Session 4

**Lithography with the advanced binary film photomask**


Superior lithographic performance of the Advanced Binary Film (ABF) photomask by HOYA has been examined by exposure experiments at 193nm and by supporting optical simulations. The results, obtained by theoretical studies and a series of irradiation experiments, show the advantages of the binary photomasks with the ABF of thin opaque layer.

In leading edge lithography for dense lines, the advantages brought about by a phase shifting mask (PSM), is moderated by the compensation of neighboring image contrasts. For the lithographic layers for small features, photomasks with binary opaque films are widely used to obtain the best lithographic performance available. At lithography for small features, it is also known that three dimensional effects reduce the contrast of aerial pattern images. A thinner opaque film on the photomask is predicted to produce higher fidelity of lithographic images.

A series of experiments using the photomasks with ABF predicts the improvement of pattern fidelity brought about by the thin film. The optical properties of the photomasks with ABF present no distinct inferiority compared to those found with the currently available binary films.

Another superiority of the ABF photomask is its durability against ArF irradiation. It is widely known that the patterns on photomasks used in ArF lithography degrade over long-term exposure. Oxidation, migration or some other chemical reactions degrade the profile properties of patterns on the photomasks. The photomask using ABF shows an extraordinarily high ArF durability. In an experiment over long-term exposure, no sign of film degradation is observed in the photomask with ABF.

The above studies confirm that ABF is a promising solution to the total requirements of the photomask with a binary opaque film for leading edge lithography.

Lithographic properties obtained by simulation and by exposure experiments are presented. The superior durability through ArF exposure is also shown.
Understanding the trade-offs of thinner binary mask absorbers


Mask topography is only one of the challenges for extending 193nm immersion lithography to 22nm and beyond. Migration to binary but thinner mask blanks, from the previously employed attenuated PSM mask technology, traded a tolerable loss in contrast for better mask making performance and reduced EFM impact [1]. The relentless improvement of reticle manufacturing required to enable 22nm technology, however, continue to drive the dimensions of mask features deep into sub-wavelength scale. In this regime, residual mask EMF effects can still degrade the imaging performance of critical mask patterns, often in the form of feature-dependent biasing and shifts of the plane of best focus that shrink the common process window and magnify the impact of mask errors.

In this paper we investigate the potential benefits in EMF effects mitigation provided by further thinning the mask absorber to the minimum possible while retaining the required opacity. This study was motivated by the narrower process variability bands observed for 22nm structures with high EMF sensitivity, when computed with rigorous EMF simulations using a thinner absorber. Resist measurements on wafers exposed with the same EMF sensitive structure built on either the standard binary blank or the thinner sample, confirmed the lower sensitivity to mask topography of the latter while also providing a significant process window improvement. We further observed that thinner topography allowed for a smaller mask bias, resulting in improved mask manufacturability with less potential for mask corrections to be limited by mask manufacturability rules such as small assist features and small corner to corner gaps.

Thinning the absorber, however, is typically accompanied by an increase in reflectivity of the mask blank which may influence the nature of stray light in the imaging system. To understand the consequences of increasing the blank reflectivity, a double expose scheme was used to measure stray light and determine the relative contribution from the imaging system optics, the mask blank reflectivity, and pellicle thickness. Initial results show that the increased reflectivity of the thinner blank has minimal impact on stray light effects in the scanner and that the overall mask reflectivity at high angles is typically dominated by the pellicle thickness.

In this paper we will also explore other relevant characteristics of these novel mask blanks, such as diffraction efficiency, EMF-induced focus drift, changes in contrast, and the implications for increased reflectivity, radiation damage response, smaller assist feature size and resist model calibration. These results will be demonstrated with both rigorous electromagnetic simulations and experiments on a set of EMF sensitive structures for 22nm contact and metal layers, while simultaneously verifying that the imaging performance of the remaining patterns is unaffected. The use of thinner blanks also improves the mask making process, contributing to better mask CD uniformity and overall better lithographic performance as discussed in [2].


Aging study in advanced photomasks: impact of EFM effects on lithographic performance with MoSi binary and attenuated PSM 6% masks

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The mask dimensions continue to shrink to meet the ITRS roadmap. With the extension of 193 nm immersion lithography, the masks are subjected to electromagnetic field at high NA and aggressive k1 whose effects are now significant. Signs of absorber degradation have been recently shown during long term 193 nm exposures in the subwavelength diffraction regime [1]. The damage mechanism known as Electric Field induced Migration of chrome (EMF) [2] partly contributes to lifetime reduction of advanced masks and results in progressive CD alteration, CD uniformity (CDU) degradation and OPC signatures changes. The aim of this study is to evaluate the impact and rate of absorber degradation due to intensive ArF exposures on OPC strategies and influence to through pitch process window for sub-45 nm technology nodes. Lithographic performance is characterized on 300 mm Si wafers after cumulative reticle aging stages. The aging test exposures are carried out directly on 193 nm exposure tool to duplicate the production environment. The analysis of printed wafers will be correlated to advanced mask tool. Experiments are performed on two types of reticles to compare the mask damage of conventional 6% attenuated PSM to new binary material OMOG (Opaque MoSi On Glass) reticle [3, 4]. Test patterns have been generated with and without a set of OPC model calibration structures on both masks. The layout is based on 90 nm half pitch design rules down to 40 nm hp (28 nm node). The relevant test patterns have been selected among different classes such as 1D structures (dense and isolated Line-space), 2D patterns (Line-end shortening) and complex structures (SRAM devices, H or combs patterns). We will also investigate the Sub Resolution Assist Feature (SRAF) printability through Process window, the linearity MEEF or pitch variations during aging cycles. The combination of metrology measurements between printed wafers and reticles enables to define accurately the impact of mask damage caused by EMF effects on various test patterns and CD evolution.


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Development of template and mask replication using jet and flash-imprint lithography

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7823-21, Session 4

7823-22, Session 4

7823-23, Session 5

Conference 7823: Photomask Technology
The Jet and Flash Imprint Lithography (J-FILTM) process uses drop dispensing of UV curable resists for high resolution patterning. The technology is actively being used to develop solutions for memory markets including Flash memory and patterned media for hard disk drives. It is anticipated that the lifetime of a single template for pattern transfer will be on the order of 10^4 - 10^5 imprints. This suggests that tens of thousands of templates/masks will be required. It is not feasible to employ electron-beam patterning directly to create this volume. Instead, a "master" template - created by directly patterning with an electron-beam tool - will be replicated many times with an imprint tool to produce the required supply of "working" templates/masks. In this paper, the ability to fabricate replica templates and masks is demonstrated.

In the case of patterned media, the process starts with the fabrication of a master template. An example of this process, for 25nm bit patterns, is shown in Figure 1. A high resolution electron beam resist, such as ZEP520A is used to define the bit array. After pattern transfer, a final relief image is formed in the mask. Figure 1a depicts 25nm half pitch pillars in the fused silica master. The master pattern is then transferred to a replica blank (Figure 1b). The working replica is then used to print the bit pattern array on a disk (Figure 1c).

An example of a fully patterned discrete track replica is shown in Figure 2a. The replica is a 150mm diameter fused silica wafer. In this example, the pattern includes both the media and the servo patterns (Pictured in Figures 2b and 2c). Patterning starts at a radius of 16.5mm and ends at 31.5mm. Figure 3 depicts the change in critical dimension across the radius of the disk. CD uniformity is generally well controlled, with variations occurring at the inner and outer radius of the patterned area.

The same replication process is now being adopted for semiconductor memory fabrication. In this case, a 6025 master with a 33 x 26 mm patterned area is used to transfer the relief images into a 6025 replica mask. Initial results look very promising. Figure 5a shows 32 nm half pitch lines imprinted with the master. Figure 5b shows the 32nm relief images transferred onto the replica mask.

This paper will review the process and tools used to fabricate the replicas. CD, CD uniformity, and relief image fidelity will also be discussed.

7823-24, Session 5
6-inch circle template fabrication for patterned media

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1. Introduction
Nanoimprint lithography (NIL) is one of the promising candidates for a method of fabricating a patterned media for next generation hard disk drives. The pitch, characterizing the feature size on the media, will become 40-50 nm for discrete-track media in 2011 and 25 nm for bit-patterned media in 2013. Master and replica template fabrications are the key issues in NIL technology. Silicon master template fabrication process by using two kinds resists, ZEP520A and new chemically amplified resist (CAR), have been developed at DNP. Advantages of silicon wafer are good dryETCHing capability and familiar to CAR (less quenching at interface) in comparison with quartz substrate.

2. Silicon master template process with ZEP520A resist and new CAR resist ZEP520A resist has high resolution performance and good process stability but has a problem of low throughput because of its low sensitivity when it is used at a high acceleration voltage of 80-100 kV. Both resist processes evaluation results with high acceleration voltage x-y stage and rotary stage e-beam writers will be reported from the view point of patterning performance (CD accuracy, post exposure delay, etc) and writing time. Test pattern pitches will be 50 nm and below.

3. Quartz replica NIL process with silicon master
The first trial result of S-FILTM process with a silicon master to quartz wafer was reported at PMJ2010, however it was only imprint resist pattern before resist volume optimization. Recent progress after PMJ2010, which will include quartz etching results, will be reported.

7823-25, Session 5
Inspection technique for nano-imprint template with mirror electron microscopy

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A nano-imprint-lithography (NIL) process has been proposed as a method of making patterned media for the next generation magnetic recording media. Master template accuracy is extremely important for the NIL process because the NIL is 1:1 process. Inspection tools are required to check defects and dimension accuracy of the master template. The required specifications of the inspection tools of the master template are as follows: a sensitivity to detect patterns smaller than half of track pitch, an inspection time for whole surface of the master template less than a few hours, testability of both periodic and non-periodic structures, and damage-less inspection to the master templates. Optical inspection tools and scanning-electron-microscopes (SEMs) are conventionally used as inspection tools for templates of the NIL. But they are difficult to satisfy all the specifications. In this study, we examined the potential of mirror-electron-microscope (MEM), which has higher sensitivity than the optical inspection tools and faster throughput than SEMs, as a master template inspection technique.

In MEM, the electron beam irradiates an area of 50 micrometers wide on a sample. A sample is biased with a high negative voltage near an acceleration voltage to reflect the irradiated electrons in the opposite direction at the vicinity of the sample surface. A convex portion on the surface convexly distorts the equipotential surface, and a concave portion concavely distorts this surface. The reflected electrons diverge above a convex portion and converge above a concave portion. A convex portion is displayed as a dark and larger spot than width of the convex portion when the focusing position of the lens is set above the surface. A concave portion is displayed as a bright and smaller spot when the position is above the surface. Because the MEM images reflect the configurations of the equipotential surfaces, the MEM is able to enlarge the size or enhance the contrast for the configurations of the sample surface, resulting in high sensitivity. Moreover, because the irradiated electron has little or no contact with the sample surface, the MEM is a damageless inspection technique.

We observed line and space patterns with half pitches of 50-100nm in which the width of only one line was slightly changed, using the MEM to verify the sensitivity. As a result, the MEM was detectable for the dimension error of above 3 nm in line and space patterns at 30 nm per pixel magnification. Assuming that a field of view of the MEM image is 30x30 square micrometers and the acquiring time per image is 10 ms, the inspection time for 2.5 inch whole surface of the master template is about 10 hours. Consequently, the MEM is a promising candidate for nanoimprint master template inspection due to its high sensitivity and acceptable throughput.

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7823-26, Session 6
Writing 32-nm hp contacts with curvilinear assist features

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In writing contacts at 32nm half-pitch with 193nm immersion lithography, circular main features and curvilinear sub-resolution assist
features will be desirable on masks. Using conventional methods, the best depth of focus, exposure latitude, and critical dimension uniformity on wafer could only be achieved with unrealizable mask write times. Previous papers have described a gradual improvement over the past two years to avoid this trade-off. For example, Manhattanization of the shapes generated by inverse lithography techniques has reduced the required shot count while maintaining best process windows. Using the model-based mask data preparation technique total shot count required to print such Manhattanized assist features is further reduced significantly. This paper is the first to present test writing results of 32nm-hp patterns using a conventional variable shaped beam mask writer with the new model-based mask data preparation technique. Using this new technique, best process window and improved critical dimension uniformity are achieved while demonstrating reduced shot count. SEM images of resist patterns written by a production mask writer will be shown.

7823-27, Session 6

Optimization of MDP, mask writing, and mask inspection for mask manufacturing cost reduction

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Mask Design, Drawing, and Inspection Technology Research Department (Mask D2) of Association of Super-Advanced Electronics Technologies (ASET) finished its 4-year project aiming at the reduction of mask manufacturing cost and turn-around-time. Key concept of the project is close relationship and synergism of three fields: MDP, mask writing, and mask inspection based on four key avenues: common data format, good use of repeating patterns, pattern prioritization based on design intent, and parallel processing.

We defined a data format based on OASIS that can express the repeating patterns in a way that the data volume becomes small.

We developed a flow that creates the priority of mask patterns (Mask Data Rank: MDR) based on design intent of patterns from commercial EDA tools. In mask inspection, MDR is used to control defect-sensing threshold to avoid excess inspection. We have examined that MDR can reduce review time by using some pattern data. MDR can be used to optimize writing condition such as beam settling wait time and maximum beam in mask writing. We verified the validity in mask writing also.

We developed repeating patterns extraction flow from mask pattern data after OPC. The extracted result is expressed by above mentioned common data format. It is used for character projection (CP) to reduce shot count of mask writing. We examined shot count reduction by actual data and verified writing time reduction by using mask writing simulator. We also made actual CP mask and examined writing results using e-beam writer we developed.

We developed a parallel writing e-beam system called Multi Column Cell (MCC) consists of four columns. The tool is equipped with CP capability. We examined basic performance of the system such as crosstalk between beams, beam stability and so on. We also examined system performance of the system such as resolution, stitching accuracy, position accuracy, writing speed, and so on.

In mask inspection technology, we developed a new parallel data processing circuit that can treat MDR and results of layout analysis as input data to perform variable sensitivity mask inspection. We examined the validity of newly developed function by the actual inspection of actual masks. In mask inspection, we also developed defect printability function that judges the severity of detected defects by the simulation of printed image of wafer.

Other than above developments, we developed an integrated diagnostic system for e-beam mask writer that detects irregularity of data processing, amplifier output signal, and external environments. Thus, four avenues (common data format, good use of repeating patterns, pattern prioritization based on design intent - MDR, and parallel processing) in three (MDP, mask writing, and mask inspection) have close relationship and utilized to make mask manufacturing efficient. In the presentation, results and remaining issues of the project will be discussed.

7823-118, Session 6

Generalization of shot definition for variable shaped e-beam machines for write-time reduction

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We propose a new composite aperture for shaped ebeam exposure tools. This aperture is able to print in a single shot a parameterized more general shape commonly found in post correction layouts. The aperture may be used in mask- and wafer-patterning ebeam tools. The physical and mechanical nature of the aperture appears to be fundamentally similar to existing apertures that form rectangular shapes, yet it reduces the required shot count for exposure by as much as half. The paper will present the concept and data preparation results based on a fracturing prototype tool. It will discuss the influence of upstream data processing and outline steps required for full implementation.

7823-28, Session 7

Physical resist model calibration for implant level using laser masks

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To reduce cost, implant levels usually use masks fabricated with laser writer, which is known to have significant mask errors. In fact, for the same implant photoresist process, Optical Proximity Correction (OPC) models have to be developed separately for the negative and positive mask tones to account for the errors in mask process. However, in order to calibrate a physical resist model, it is ideal to use single resist model to predict the resist performance under the two mask polarity. In this study, we show our attempt to de-convolute mask error from the Clear Positive (CP) and Clear Negative (CN) tone CD data collected from bare Si wafer and derive a single resist model. Moreover, we also present the predictability of this resist model over substrate complexity/variations by comparing simulated profiles against cross-section images of various features.

7823-29, Session 7

Compensation methods using a single-layer model for buried defects in extreme-ultraviolet lithography masks

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A new fast and accurate model for a buried defect in an extreme ultraviolet (EUV) lithography mask will be presented and used to develop defect compensation techniques. This model is similar to the single surface approximation (SSA) [1], but rather than assuming that a buried defect only affects the reflected phase, the new model adjusts the phase and magnitude, and accounts for off-axis incident light. The accuracy of the new model will be verified by comparisons to finite difference time domain simulations (FDTD), ray tracing [2], and the standard SSA model. The fast model will be integrated into the
simulator RADICAL [3], which means it must accurately predict the reflected field for angles of incidence much higher than the nominal angle of incidence on the mask. This new method, which is nearly as fast as the advanced SSA model presented in [3] but more accurate, is required because the assumptions made in the advanced SSA model are not adequate for RADICAL simulations of half-pitches below 32nm, and the ray tracing method is too slow for certain applications. The compensation methods will focus on off-axis illuminations, such as annular and dipole, where the mutual coherence functions cause interactions across a large area on the mask and make the development of simple compensation strategies difficult.

An accurate EUV defect model must correctly predict the magnitude and phase of the reflected electric field. The single surface approximation, which assumes the defect only affects the phase of the reflected light, is fairly accurate for simulating the reflection from normally incident EUV light on the multilayer, even if the layers are non-uniform due to multilayer smoothing. But, there are a few modifications which can be made to this model to increase the accuracy and applicability without sacrificing speed. The first is to adjust the magnitude of the reflected field in addition to the phase. If the lower layers are non-uniform the small reflections from each layer do not add in phase and the reflected magnitude is reduced. The other modifications account for the reflection of light incident at angles above the nominal angle. Increasing the incident angle above the nominal angle also decreases the resonance, causing light to penetrate deeper into the multilayer and increasing the effects of the lower layers. This penetration also causes a small horizontal shift in the position of the defect image. A new model which efficiently accounts for these effects, referred to as the single layer model, will be presented.

Buried defects less than 1nm tall on the multilayer surface near absorber lines can cause greater than 10% CD change for 22nm dense lines [4]. For smaller lines, the allowable defect height will be even shorter. It may not be possible to reliably manufacture EUV mask blanks without any defects larger than this limit, so compensation could be necessary. The goal of the methods in this work is to build upon previous compensation proposals [5] using the new single-layer model to develop techniques that are effective through focus for off-axis illuminations.

REFERENCES

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Evaluation of a new model of mask topography effects
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In the early 1990s, wafer images printed with alternating aperture phase-shifting masks exhibited a large departure from the simple Kirchoff thin mask approximation as the depth of the mask patterns was larger than the exposure wavelength. In particular, the transmission through the etched quartz regions of the mask was substantially smaller than the transmission through the unetched regions of the mask. These effects were simulated using slow but accurate methods such as FDTD and RCWA. Correction methodologies including quartz undercut and sizing were successfully implemented. Fifteen years later, the mask main feature sizes were now smaller than the exposure wavelength resulting in mask polarization effects even for binary and attenuated phase-shifting masks. With the advent of model-based OPC, a fast simulation of these effects was now necessary in order to apply corrections. One approach to account for these effects is to place additional polygons with adjustable phase and transmission along the edge of the patterns. Over the past few years, more aggressive resolution enhancement techniques such as inverse lithography and source mask optimization have been pursued. Such techniques lead to much more complicated mask patterns and the accuracy of current mask models need to be revisited.

In this paper we will review and evaluate various mask models in terms of speed and accuracy as compared to FDTD and RCWA implementations. In particular we will compare to existing approaches a novel implementation based on the creation of a separate mask model. A variety of test structures resulting from model-based OPC, inverse lithography, and source mask optimization tools will be used for this study.

7823-31, Session 7

An advanced modeling approach for mask and wafer process simulation
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A new modeling technique to accurately represent the mask and wafer process behavior is presented.

The lithography simulation can be done in three steps: i) mask simulation, ii) latent image calculations and iii) resist process simulation. The leading edge designs, such as 32 nm and beyond, require higher-fidelity models to adequately represent each of these actual processes. The effects that are previously considered secondary, have become more pronounced at the advanced technology nodes.

The mask distortion issues due to the limitations in manufacturing can be modeled ahead of time and can be included in the design of layouts to achieve a better optimization. The mask model has two main components: material and manufacturing effects. For the material effects the EMF-grade solvers perform well but the computational requirements are heavy. Similarly, the manufacturing effects have always been approximated to a certain degree. In this work, we present an adaptive nonlinear mapping algorithm that models the remaining effects that are not modeled by the existing approximations.

The wafer distortions may be due to the limitations in the optical system, as well as to the properties of the resist and development process. Among the various effects, the post exposure bake and development process model mismatches, once considered negligible, need to be addressed even for the OPC tasks for the advanced nodes.

Our modeling approach combines two components: Physical models and nonlinear mappers. To model the physical phenomena we use separate models, some of which were presented in [1-5]. For the behavior that is not completely captured by these physical models, we developed an adaptive nonlinear mapping algorithm.

The physical model parameters were calibrated by a genetic algorithm whose details were outlined in [1]. The nonlinear mapper model parameters were identified by a gradient descent method. The final paper will demonstrate the improvement using the real process data.

Given the computational requirements for a practical solution, our approach uses graphics processors as well as CPUs as computation hardware.

REFERENCES
Attaining the 11-nm node using nonlinear 193-nm exposure addition of interference lithography generated pattern and projection lithography produced line-break patterns that are optimized through source-mask optimization

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Through linear or nonlinear addition Interference-Assisted-Lithography combines at least one relief image of a unidirectional grating with line-break exposures to form a two-dimensional circuit layer pattern. (1, 2, 3, 4) The grating produced may be made using optical projection or interference lithography. The line-breaks may be formed using interference lithography, high resolution optical projection lithography or direct write. Sidewall frequency quadrupling techniques can extend 193nm optical projection lithography to the 11nm technology node and beyond. Using hyper-numerical aperture, optimized extreme off-axis illumination with TE-polarization, weak PSM and negative-acting resists line-break patterns can be produced with better than 0.3 micron depth-of-focus with 5% exposure latitude and maximum exposure latitude of greater than 15% at best focus. (5) Large depth-of-focus across-pitch range solutions for 50nm line-break patterns require the use of multiple exposures with conventional off-axis illumination however using unique sources the imaging process may be reduced to fewer even single exposures. This work defines possible integrated imaging systems that will allow imaging of deep sub-wavelength sized line-break patterns and then compares these to other solutions that have been proposed in the literature. Specifically, inverse lithography Source-Mask Optimization (SMO) (Gauda ref) is used for the development of across chip line-break primitive solutions that through non-linear addition will be combined with uni-directional gratings.


7823-33, Session 8

Model-based double-dipole lithography for sub-30-nm node device

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As the optical lithography advances into the sub-30nm technology node, many candidates of lithography have been discussed. Double dipole lithography (DDL) has been a primary lithography candidate for a merit of simple process and a low mask cost compared to the double patterning lithography (DPL). However, new DDL requirements have been also emerged to improve the process margin and to reduce the mask-enhanced error factor (MEEF), which is to maximize the resolution and image contrast. There are two approaches in DDL such as model based- and rule based-DDLs. Rule-based DDL, in which the patterns are decomposed by the simple rules such as x- and y-directional rules, shows the low process margin in the 2-dimension (2D) patterns, i.e., line-end to line-end, line-end to bar and semi-isolated bars.

In this paper, we first present various analyses of our new model-based DDL (MBDDL) method. Our goal is to maximize the process margin of the 2D patterns. Our main contributions are as follows. (1) We generate new 2D test patterns including various configurations of the metal layer. The new 2D patterns can be used to optimize the parameters of the MBDDL and to build the good design rules. Even though the parameters of the MBDDL are optimized, it is hard to improve process margin in the patterns with low margin. Therefore we exact the design rules to implement the MBDDL. (2) We optimize the initial layout decomposition, which is the first step of MBDDL and affects the whole of MBDDL quality. In addition, the decomposition of MBDDL is applied with the process-window OPC (PWOPC) in terms of the criteria of edge placement error (EPE) and mask rule checking (MRC) violation. Our new model-based approach including the newly designed test patterns and optimized decomposition parameters leads the improved the depth of focus (DOF) and enhanced the exposure latitude (EL). We achieve the 80nm DOF and 8% EL, which are manufacturable margins for the bi-direction metal-1 with 80nm pitch.

7823-34, Session 8

SMO mask requirements for low-k1 lithography

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To keep pattern shape fidelity with reasonable process windows in low k1 lithography is getting more and more difficult as the k1 decreases [1-2]. Source-Mask co-Optimization (SMO) is the key technology to realize good pattern fidelity with wide process windows for a wide variety of logic patterns [3-8]. In the SMO, different levels of source and mask complexity can be set for the optimization. In general, the increased freedom of the mask shape yields better process windows especially for more isolated patters with SRAFs by approaching to the ideal mask shape suggested by SMO tool [6]. However, with increasing mask complexity, mask writing time increases greatly and mask inspection becomes more difficult. Therefore, it is very important to have the strategies to balance the lithography performance and mask cost, based on the understanding of current mask manufacturability and inspection capability.
This paper tries to clarify the current status of mask manufacturability and inspection capability for complex SMO masks for low k1 technology nodes (28 nm and beyond). This paper also investigates proper CD requirements for the SMO masks with different mask complexity levels with either rectangular or free form SRAFs. For the investigation, SMO masks are prepared by multiple mask vendors with a variation in blanks and mask complexity levels. Then wafer exposures are done with FlexRay illuminator on ASML XT:1950i. From the results, we investigate the effect of SMO mask shape on lithography performance. We also clarify the effects of mask CD variation on patterned CD using rigorous simulation. The approach to prevent the SRAF ‘printability’ is discussed in detail. From the results, we explore the proper requirements for SMO masks. This work also explores the methodologies of mask inspection for complex SMO masks based on the effects of CD differences on lithography performance.


7823-36, Session 8

A systematic study of source-error influence on source-mask optimization

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Source Mask Optimization (SMO) technique is an advanced RET with the goal of extending optical lithography lifetime by enabling low k1 imaging [1,2]. Most of the literature concerning SMO has so far focused on PV (process variation) band, MEEF and PW (process window) aspects to judge the performance of the optimization as in traditional OPC [3]. In analogy to MEEF impact for low k1 imaging we investigate the source error impact as SMO sources can have rather complicated forms depending on the degree of freedom allowed during optimization.

For this study we use tachyon SMO tool on a 22nm metal design test case. A complete free form and parametric source solutions are obtained using MEEF and PW requirements as main parameters. For each type of solution a forced deformation of the source is then introduced to study the impact on the previous criteria. Based on the findings we conclude on the choice of freeform or parametric as a source and the importance of source error in the optimization process.


7823-37, Session 8

Impact of model-based fracturing on proximity effect correction methodology

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Extending 193nm immersion lithography using single exposure is forcing the industry to move to more and more complex resolution enhancement techniques such as inverse lithography and source mask optimization. These techniques require extremely complicated mask shapes that can lead to mask write times exceeding 24 hours for advanced nodes. Inverse lithography solutions generally yield curvilinear mask shapes that have been approximated by “Manhattan” layouts in order to reduce the mask write time. Such approximation tends to preserve the overall process latitude, but reduces accuracy as the MEEF is increased as the perimeter of the features is increased [1]. Model-based fracturing [2,3] has been proposed as a way to better replicate the curvilinear shapes on the mask while reducing the number of shots and thus reducing the overall write time. To achieve low shot count and accurate mask image, more degrees of freedom are available if the shots can be overlapped and further if the dose can be assigned for each shot individually. Unfortunately, this departure from current VSB tool writing strategy breaks some of the assumptions made for proximity effect correction. For example shots generated during the model-based fracturing step do not necessarily represent the target mask image anymore.

In this paper two solutions to this problem will be reviewed. The first solution consists of modifying the proximity effect equations and using the new equations to calculate the dose for each shot. The second solution makes the correction a part of the model-based fracturing process.
Fast pixel-based OPC algorithm based on nonparametric kernel regression

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Resolution enhancement techniques such as Optical Proximity Correction (OPC) are extensively used in today’s semiconductor manufacturing industry. OPC approaches can be broadly classified into rule based and model based. One approach to model based OPC is component based OPC (CBOPC) whereby we decompose a layout into components such as edges, convex corners, and concave corners, and then optimize the positions of these components using mathematical models to represent the image formation process of the optical lithography system. Another approach to model based OPC is to optimize the layout at the pixel level and to optimize the values of the binary or non-binary pixels using similar models as before. This is also known as Inverse Lithography Technology (ILT). Generally, the resulting layouts in the pixel based OPC (PBOPC) are more complex to manufacture than the CBOPC, but they also result in more desirable wafer intensity patterns. This is because PBOPC has many more degrees of freedom to optimize than CBOPC.

To speed up convergence of CBOPC, Gu and Zakhor recently proposed a fast, linear regression approach in order to arrive at the initial direction of movement of components within a layout. Subsequently Gao et al. generalized the linear regression approach to principal component analysis. While these approaches reduce the number of required iterations by 25%, they cannot be directly applied to PBOPC. This is particularly unfortunate, as the computational complexity of PBOPC is considerably higher than that of CBOPC.

In this paper, we apply a class of machine learning algorithms in order to develop fast algorithms for PBOPC. In contrast to the earlier work which uses parametric regression to estimate parameters of the function that relates input to output, in this work, we apply non-regression methods, in which regression function itself is directly estimated from the data. Specifically, we opt to use non parametric kernel regression method to estimate the output pixel values based on the input data and the training examples. In essence the kernel function, in our case a Gaussian, measures the similarity between the input and the training patterns in order to construct the output by weighted linear combination of the training patterns. Thus, our approach consists of two distinct phases; in the training phase, we collect training examples for three classes of components, namely convex corners, concave corners and edges. The training examples consist of a set of pre-OPC patterns, and their associated pixel based OPC pattern as computed by an optimization engine, in our case a commercially available software package. In the second phase, the test layout to be optimized is divided into three classes of components, and the non-parametric kernel regression is applied to each class separately. Finally, the regressed results are stitched up to compose the final PBOPC pattern. Unlike previous regression approaches, this output does not require additional iterations. Our proposed algorithm is shown to improve the speed of a current commercially available PBOPC software package by a factor of 3 to 7 with similar or lower error performance.
Fundamentals and applications of dry CO\textsubscript{2} cryogenic aerosol for photomask cleaning

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CO\textsubscript{2} cryogenic aerosol cleaning is a dry, residue-free and chemically inert technique that has been well established for a wide variety of surface cleaning applications such as Si wafer, photomask, MEMS devices, packaging fabrication, imaging devices, metal lift-off, ion implanted photosist stripping, disk drives, flat panel displays, and Post-dicing for 3-D stacked IC integration flows. The CO\textsubscript{2} cleaning technique doesn’t suffer from disadvantages of current wet-cleaning techniques such as transmission/phase loss, CD loss, haze/progressive defects, and limitation on number of cleaning cycles. The technique is based on formation of a CO\textsubscript{2} cluster with forward momentum plume due to the sudden expansion of liquid through a well-designed and optimally-shaped orifice. The plume can be aimed at adsorbed contaminants to detach and be transported away from its site through either the gas phase or sliding on the surface. The major challenges using the technique are, a) creation of CO\textsubscript{2} beam of particles with properties that remove all unwanted particles/contaminants efficiently without damaging the fine sub-resolution assist features (SRAFs) on Photomasks, b) determination of the CO\textsubscript{2} beam purity that restricts additional contaminants from the CO\textsubscript{2} source, c) maintaining the ideal environmental condition and airflow in the cleaning chamber, such that any removed contaminants/particles are restricted from re-depositing on the active area of the mask, as well as, restricting any possible contaminants from cleaning chamber hardware from transporting over to the active area of the mask. In this paper we present the nucleation rate formulation based on Frankel derivation and growth theory for calculating the density and size distribution of CO\textsubscript{2} clusters. The formation of clusters in size, velocity distributions and their density of CO\textsubscript{2} along the long axis of plume are measured by Phase Doppler Anemometry (PDA). Based on experimental observations and analysis of the results, we have designed and applied a host of nozzles for removing contaminants for many applications including post-AFM repair debris on Photomasks. We will discuss the influence of the particle size, velocity, flux, and momentum of CO\textsubscript{2} clusters formed as expanding from the nozzle on removal probability of adsorbed contaminants as well as stress exerted on the structures. We will show that the distributions are controlled by the detailed nozzle design shape, size and surface finish. We are thus able to utilize our knowledge of the CO\textsubscript{2} process to design nozzles to widen the cleaning process window for Photomasks without any damage to the weak SRAFs. This capability has been experimentally proven for SRAFs as small as 45nm wide by 73 nm tall as well as high aspect ratio features like 52nm wide by 145 nm tall. This extends CO\textsubscript{2} cleaning technology out to 2014 for 28 nm DRAM half pitch node. Some foreign material adder contaminants (FMNR) that were not removed by PoR Wet Clean were removed by the CO\textsubscript{2} cryogenic aerosol technique.

Inspection solutions for EUV-mask defectivity applications

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The first generation EUV full-field scanning systems will roll out to the end-users for early learning starting 2011. These systems are specified at 60wph throughput, giving the users a chance for implementation at the 22nm node.

While the source and resist questions were the #1 concern in the past, EUV mask defectivity is now being recognized as the primary challenge of this EUV program, and, is under close investigation in all advanced mask-shops. The mask inspectability challenges are mapped, and equipment manufacturers are challenged to develop appropriate solutions to all defectivity problems. These applications start at blank production, for detecting buried phase defects and top contamination, followed by patterned mask inspection for absorber defects, and subsequent contamination and CDU inspection for final qualification.

In this paper we summarize the studies and present the results of developing solutions to all EUV mask inspection applications, for the early learning phase down to 22nm HP node, using 193nm advanced imaging mask inspection technology. This work includes new results from 22nm EUV masks, phase defects and contamination on a blank mask, and sensitivity enhancement techniques.

Mask process correction (MPC) modeling and its application to EUV mask for electron-beam mask writer EBM-7000


Semiconductor scaling is constantly pursued to fabricate lower power and higher performance devices. One of the lithography technologies strongly following this trend is EUV to take advantage of its short wavelength. SEMATECH A-projection has shown that EUV lithography will start in around 2013 at last Photomask Technology (BACUS2009), although EUV lithography still has such issues as light source, defect free blanks and defect inspection to be overcome to be used for production. In parallel with the efforts of resolving these issues, it is to be noted that the difficulties in patterning with minute feature sizes like hp 22nm/16nm are getting significantly important and required extremely high accuracy.

CD linearity of EUV mask, written by electron beam mask writer, does not have simple signatures like the conventional COG (Cr on Glass) masks do, it has been reported. Such a symptom is caused by scattered electrons form EUV mask itself which comprises stacked heavy metals and thick multi-layers.

EB mask writer, EBM-7000 (NuFlare technology Inc.), has certain functions to compensate for pattern/CD errors incurred by proximity effect, fogging effect and loading effect with dose modulation. It is assumed that those effects have several dozen um to a few mm in their impact length. On the contrary, range of scattered electrons of EUV mask is a few um or less. Therefore, even if those functions are applied to suppress errors of CD linearity on EUV mask, accurate correction will not be achieved within allowable time because of in-adequate calculation grid sizes. They should be 1/100 -1/10 smaller for EUV mask. Also, every pattern should be divided into small shot sizes to fit the grid sizes to which respective dose settings are assigned to meet high accuracy. Then, the number of shots will increase substantially to cause the writing time so long.

To overcome this issue, Mask Process Correction (MPC) will be ideally applicable. This technology was already presented for correction of CD non-linearity on COG mask (ex, Yasuko Saito et.al, Brion technologies, PMJ2010). Every pattern is reshaped for correction in MPC. Thus, it is expected that the number of shots would not increase maintaining the writing time within the reasonable range. In this paper, MPC is extended and applied to modeling to correct CD linearity errors on EUV mask. And its effectiveness is verified by simulations and experiments through actual writing test. These results will be reported.
Sensitivity results from a 193-nm EUV-mask inspector

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Reticle quality and the capability to qualify a reticle are key issues for EUV Lithography.

We expect current and planned optical inspection systems will provide inspection capability adequate for development and production of 2X hp masks. We illustrate inspection sensitivity results using the ToronTM 610, an advanced 193 nm mask inspection system, through measurement of standard EUV programmed defect masks.

Building upon work that we published at the SPIE Advanced Lithography Conference in Feb 2010 [1], we show data from a series of EUV programmed defect masks. We illustrate the influence of EUV absorber design for 193 nm optical inspection, including comparisons between a Booster, an anti-reflective coating, and a bare TaN absorber stack. Working closely with leaders in EUV mask development, we explore the optimization of absorber stack design for mask inspection, mask process and cleaning, and EUV lithography.


Study on storage components and application performance for mask haze prevention

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The amount of sulfate ion on mask surface will increase haze defect growing once exposed by an ArF laser. Our evaluations used extraction method and IC test to examine the amount of ions for current mask storage pod included the material of ABS, PMMA, PC, PC+OF, PC+CNT, PEEK and LCP. Moreover, Moreover, PSM (Phase shift Mask) haze lift time and dosage was also interrelated with the amount of chemical contaminant aggregation for storage pods. Also, we used the impinger and Cr Blank IC test to verify the best condition for different storage conditions. Resulting from our investigations, we applied different mask types to different mask storage pods and tools in order to keep free haze performance base on cost consideration. Consequently, the optimization components of mask types and storages will contribute the enormously economical benefit.

An analysis of correlation between scanning direction and defect detection at ultra-high resolution


As the design rule of wafer has been shrinking, mask CD is still at the stage of decrease. In a field of ultra high resolution, most of mask inspection adopt TDI(Time Delay & Integration) sensor to minimize the inspection cost. Because the most of defect is a variety of rectangular shapes, sensitivity of TDI sensor and outbreak of false defect is influenced by the pattern size, shape and direction of forming; that arise from scan direction. We manufactured ArF and EUV mask inserted the programmed defect, the minimum size of 64 nm (criteria of mask), and evaluated the correlation between scan direction and defect size/shape experimentally. At first, we proceeded to the mask inspection with the direction of parallel to long side of rectangle. Later, we did the identical inspection with the direction of perpendicular to long side or rectangle, and we compared each other. Finally, we could detect the minimum size of 80nm defect, and found the mask inspection with the parallel direction to rectangle's long side increased sensitivity of TDI sensor. In addition, we enumerated the emerged problems in order to support collaborative goal of ultra high resolution.

Feasibility study of EUV patterned mask inspection for the 22-nm node

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Extreme Ultra Violet Lithography (EUVL) is a major patterning solution candidate being considered for the ITRS (International Technology Roadmap for Semiconductors) advanced technology nodes commencing with the 22nm Half Pitch (HP) nodes. Achieving defect free EUVL masks is a critical issue in and thus the importance for mask inspection technology to be ready to support pilot line development. EUV mask inspection presents additional challenges with smaller line width, multilayer defects and no pellicle to protect the mask. In addition, Line Edge Roughness on the mask can limit the detection sensitivity. Configurable inspection illumination conditions were considered to enhance the contrast of the mask image and improve the detection sensitivity.

Here we present experimental results of evaluating the defects detecting capability on several EUVL masks. These results are generated by inspecting EUVL masks using a DUV (193nm) reflected illumination optical inspection system.

Free form micro-lens arrays enable innovations and more efficiency for mask inspection tools

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The semiconductor industry follows Moore’s law for more than 40 years, achieving year after year smaller and smaller structures. It would not take long till the steppers achieving sub 20nm node would be ready to be transferred from the research and development divisions to production line. Not only wafer structure is getting smaller. High demands on the other components increases as well. Masks follow trying to get along with their structure as small and as precise as possible. All optical elements should get more out of their function, like efficiency, intensity stability and durability.

This makes a great challenge for a metrology, which has to be able to inspect quality of photomasks used in exposure tools. These challenges are getting higher as structure is getting smaller. That brings high demands on the inspection systems and one of their major features: illumination of the inspected element. The illumination should show almost no inhomogeneity and most likely some specially defined far field distribution.

LIMO’s unique production technology based on computer-aided design enables the manufacture of high precision asphere arrays. These free form micro-optical cylindrical lens arrays enable special intensity distribution, as well as highly homogeneous illumination with inhomogeneity less then 1% (peak to valley). Micro-optics arrays consisting of cylindrical lens arrays provide separate manipulation of the light distribution in x and y axis. With fill factors close to 100% these optics are extremely efficient. They can be manufactured in broad variety of materials. Fused silica or calcium fluoride enables high transmission and long life durability of these optical elements.
Due to the special free form such as asymmetric profile these lens arrays can offer extreme uniformity far field at the target non orthogonal to the illumination path. The feature under inspection can be uniformly illuminated even if it lies at a specific angle to the illumination.

Application results of such micro-lens arrays are presented for beam shaping of high power diode lasers. The generation of a homogeneous light field by a 100 W laser with tilted illumination at an angle of 55° is shown. Homogeneity of better than 95% was achieved for a field size of 300mm x 340mm.

Every single micro-lens of the lens-array can have its own profile and aperture. Thus special intensity distribution such as simultaneous multiple uniform non-equidistant spot generation can be achieved. Several types of uniform spot generation based on different simulations are presented.

**7823-89, Poster Session**

**Strategies for future inspections**

S. Mangan, Applied Materials (Israel)

While the EUV program seems to take off, there are new concepts to lithography which suggest that EUV may not be alone. The increasing costs of lithography may drive the manufacturing into mixed solution, using multiple patterning in ArF, EUV, nano imprint or direct write. This diversity will impose a huge challenge to mask and wafer inspection, since there will be no single solution of one-fits-all.

Here we discuss the inspection strategies on several scenarios of future mask technologies, from EUV to mask-less. Here, we review different inspection technologies for EUV technology, and present results from preliminary studies using some of these technologies. We present and compare results from fast EBI and 193nm DUV studies, and discuss their different roles for EUV litho and alternative technologies.

**7823-90, Poster Session**

**28N foundry reticle requal challenges and solutions for IC fabs**

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Most leading-edge IC fabs continue to use direct reticle inspection for “early warning” of haze defects before they print on wafers. This inspection strategy enables fabs to cost-effectively maintain the highest yield possible. As foundry IC design rules advance from 45/40 nm nodes to 32/28 nm, mask patterns continue to shrink in size and increase in pattern density. More layers are exposed on 193nm immersion scanners, and as a result, reticle requal inspection requirements become more challenging in order to meet requirements for sensitivity and inspectability performance.

In this paper, we examine the primary reticle requal inspection challenges 32/28 nm logic mask designs present. Inspection issues for the existing STARlight 2+ industry-standard inspection algorithm caused by more aggressive SRAF and higher MEEF mask designs are first examined. A new and improved algorithm to support requal requirements for these advanced nodes is then introduced and tested. These data are analyzed to evaluate the overall inspection capability and sensitivity of the new algorithm to meet 32/28 nm foundry reticle requal needs for high-volume production in IC fabs.

**7823-91, Poster Session**

**Study of EUV-mask inspection technique using DUV-light source for hp-22-nm node and beyond**

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EUV lithography with 13.5nm exposure wavelength is dominant candidate for the next generation lithography because of its excellent resolution for 22nm half pitch (hp) node device. We have already developed the mask inspection system using 199nm wavelength with simultaneous transmitted illumination and reflected illumination optics, which utilize p-polarized and s-polarized illumination for high defect detection sensitivity, and is an effectual candidate for hp 32nm node mask inspection. It was produced by NuFlare Technology (NFT). Also, it has high defect sensitivity because of its high optical resolution, so as to be utilized for leading edge mask to next generation lithography.

But, applying 199nm optics to complicated lithography exposure tool option for hp2x nm node and beyond, further development such as image contrast enhancement will be needed. We developed a new image contrast enhancement method which changes the digitizing rate of imaging sensor depending on the signal level. Applying this method to actual inspection machine, we confirmed the signal contrast enhancement for fine-pitch pattern without sacrificing inspection time. By implementing the function to the inspection system, signal contrast improvement is evaluated for hp22nm defect detection. To optimize the inspection system configuration, the image detection optics with super-resolution method (p-polarized and s-polarized illumination) and the lower noise image acquisition system are incorporated in this tool. Both of reflected beam image the pattern on TDI (Time Delay Integration) sensors. To provide appropriate and effective super-resolution potential to the inspection machine, illumination type and pupil control are adjusted, the most qualified defect detection sensitivity can be achieved. Also, we evaluate the mask structure which improve the image contrast and defect detection sensitivity. EUVL-mask has different configuration from transmitted type optical-mask. It is utilized for reflected illumination type exposure tool. Its membrane structure has reverse contrast compared with optical-mask. This nature leads image profile difference from optical-mask. A feasibility study was conducted for EUV mask pattern defect inspection using DUV illumination optics. The image signal profile change by slight difference of mask pattern duty and shape, and so on. Mask structure, such as absorber reflection rate and absorber height, is important for EUV mask pattern image contrast using DUV tool. Pattern image contrast is influenced not only L/S size but also duty ratio, absorber height, reflection rate and pattern profile. Moreover, polarization condition of inspection optics illumination changes pattern image profile. Consideration of modified illumination effect is crucial for image contrast enhancement. A captured image simulator has been developed to study the polarized illumination performance theoretically of our inspection system. The simulator accurately models inspection optics including the pixel size of TDI image sensor. The interaction of light with mask features is calculated rigorously using RCWA (Rigorous Coupled-Wave Analysis) method. Image contrast enhancement effect is evaluated by P-to-P (= Max - Min) value. Preferable mask structure for defect detection with p-polarized and s-polarized illumination and possibility of miss defect detection are considered.

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Efficient MDP automation system linkage and verification focusing on Boolean layer generation
G. Shiau, United Microelectronics Corp. (Taiwan)

In semiconductor industry, with each new advanced technology node there is an increase in the number of mask layers requiring Boolean operation and verification. This increases not only mask cost but also the time spends on the mask data preparation (MDP) flow, which is already a lengthy portion of the production flow. Most critical or implant layers of new advanced technology nodes also end up with more complex Boolean equations relative to previous generations slowing the tape out flow even further. Therefore, developing an efficient MDP automation system and verification of Boolean layers instead of manual operation with high risk is necessary. In this paper, it shows that Boolean operation writing rule unification and automatic linkage between MDP related systems with verification. Finally, automatic output post Boolean data through “Automatic Boolean Creation (ABC)” program code. The manual handling Boolean operation is elimination. It’s work for reducing mask making error due to incorrect boolean operation.

MDP arrangement with mask suppliers for rising OASIS tape out
E. Deng, R. Lee, United Microelectronics Corp. (Taiwan)

In spite of few tape-out cases than those using GDSII format currently, OASIS format is GDSII's successor and is the new workhorse of IC design and tape-out area. As lots of DFM solutions appear for design rules shrinkage, output data sizes through DFM tools become larger remarkably and make a heavy load of file transfer and data preparation. Due to its compact data structure, OASIS format could form smaller files and “process blur” which means the dimension variation caused by scattering range is thought as shorter. This figure includes beam blur with resist molecular and substrate atoms scatter, and expose unintended position. The short range scattering caused by resist molecular is called as forward scattering, and the long range scattering caused by substrate atom is called as back scattering.

In 50keV VSB (Variable Shaped Beam) mask writer, usually used for mask writing, it is assumed that forward scattering is less than 50 nm, and back scattering is approximately 10 um. Actually the forward scattering range is thought as shorter. This figure includes beam blur and “process blur” which means the dimension variation caused by development process. It is difficult and not so beneficial to divide these factors, they are treated as 50nm blur. The back scattering affects to the dimension variation at this time. Line width become wider in dense area, smaller in sparse area. Thus, reasonable strategy for proximity effect correction can be like the following.

Firstly, it divides whole chip into 1um or smaller meshes, and calculates densities in each mesh. Secondly, applying Gaussian filter to the density map to obtain effective backscatter intensity. Finally, it calculates optimum exposure intensity for the patterns which belongs to the density map to obtain effective backscatter intensity. Finally, it calculates optimum exposure intensity for the patterns which belongs to the density map to obtain effective backscatter intensity. Finally, it calculates optimum exposure intensity for the patterns which belongs to the density map.
Thinking about EUV mask fabrication. It requires 64nm patterning in 4x size, when we try 16nm line width. If the forward scattering is 40 nm, its effect will appear in this feature size. Additionally, it may require smaller assist features. The way of proximity effect correction mentioned above does not concern forward scattering. This can be obstacle for down-scaling.

In this communication, we describe about proximity effect correction software which solves this forward scattering problem.

It is difficult to concern and compensate local behavior by forward scattering and global behavior simultaneously. We have developed proximity effect correction software by completely model based approach. It has worked very well, but higher speed is required.

The prior system handles two factors simultaneously. Forward scattering calculation requires of each individual patterns’ information, but the reference range is small. On the other hand, back scattering calculation needs broad area density information, but individual pattern information is not required.

In time, we take the way that compensate forward and back scattering separately, and combine the results finally. And its processing speed and compensation accuracy will be presented.

**7823-96, Poster Session**

**An optimized OPC and MDP flow for reducing mask write time and mask cost**

E. Yang, C. Li, Semiconductor Manufacturing International Corp. (China); Y. Zhu, Mentor Graphics Shanghai Electronic Technology Co. (China); E. G. Guo, Semiconductor Manufacturing International Corp. (China)

Inevitably, post-OPC layouts become more complicated because those techniques invoke additional edge, or fragments prior to correction or during OPC iteration. As a result, jogs of post OPC layer can be dramatically increased, which results in huge number of shot count after data fracturing. In other words, there is trade-off relationship between data complexity and various methods for OPC stability.

In this paper, those relationships have been investigated with respect to several technology nodes. The mask shot count reduction is achieved by reducing the number of jogs with which EPE difference are within pre-specified value. The effect of jog smoothing on OPC output - in view of OPC performance and mask data preparation - was studied quantitatively for respective technology nodes.

**7823-97, Poster Session**

**Ellipsometric investigation of mechanically polished sitall and quartz glass**

O. Shestopal, National Taras Shevchenko Univ. of Kyiv (Ukraine)

Optical materials, such as sitall and quartz glass, are used as substrates for deposition of the semiconductor active films elements and nanostructures. The samples of sitall and quartz glass were made by the special technology of the deep polishing.

The ellipsometric investigations were carried out on a 632,8 nm wavelength. In the process of measuring the ellipsometric parameters such as a phase shift between the orthogonal components of the polarization vector and an azimuth of the restored linear polarization were determined at the different incident angles $\Delta$. The measurements of $\Delta$ and $\Psi$ were made nearly the Brewster angle of the materials.

For interpretation of the experimental results the model of the homogeneous dielectric layer on the dielectric substrates was applied to the polished layer on the sitals and the quartz glasses surface. The refraction index $n$ and the thickness $d$ of the polished layer were determined by calculation using an automated program.

Within the framework of the used model, the appropriate values of refraction index and thickness of the surface polished layer were obtained: for the standard of sitall of $n=1.5365$, $d=303$ nm, for the standards of quartz glass of $n=1.454$, $d=238$, $245$ nm.

It is necessary to emphasize that the refraction index of the polished layer of sitall was appeared to be greater than the refraction index of the substrate. For quartz glass there is an opposite situation. There are two factors which can influence the value of index of refraction of the polished layer namely:

1) the local high tensions lead to the increase of the refraction index throughout the compression of a base material; and 2) a metal ions lixiviation with the polishing suspension leads to the decrease of the refraction index in the surface layer.

The total value of the refraction index is determined by correlation between the actions of these two factors.

**7823-98, Poster Session**

**Thin film metrology by FFT using SE and SR signal**

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We report thickness measurement method in semiconductor fabrication, photo, CMP process etc. Conventionally, the FFT (Fast Fourier Transform) method is applied for thick film (>1000A) with SR (Spectroscopic reflectometer). However, FFT is not able to apply thin film (<100A) region with SE (spectroscopic ellipsometer) and SR since interference between the film layer is not made. We report thin film (<100A) measurement FFT method. This can use with not SR but SE signal. Conventionally, FFT method have limitation thin film and SE signal analysis, here we report our experiment FFT application to thin film SE signal and possibility of measurement. Theoretical viewpoint, the SE and SR signal contain the thin film information but FFT algorithm can’t interpret the FFT peak to film thickness so we show several peak have film thick information. And SR reflection equation is simple relative SE Psi and SE delta equation, so we have solved SE Psi and Delta equation can be applied to the FFT calculation. We easily show the SE signal can be applied to FFT. Experimental viewpoint, SE-signal is used FFT and have correlation between FFT peak and film thickness. We expect this FFT-based metrology applicable to not only film but also pattern measurement i.e., CD (Critical Dimension) and SWA (Side wall Angle) etc. measurement because pattern information is contained the SE and SR signal. FFT method is powerful that can measure complex structure region, such as, 3D Gate, vertical stack, double-, triple-, quad- pattern. The complex film and pattern region, the conventional method such as, WAVE (wollam Co.) ans Optical - CD method is hard to stack and pattern modeling, respectively.

**7823-99, Poster Session**

**A new CDSEM metrology method for thin film hardmasks patterns using multiple detectors**


Thin film hardmasks with 10 nm or less are used in double patterning techniques to generate fine patterns for 32nm-node and beyond. Using a CDSEM for high accuracy measurement of these thin film hardmasks line patterns is difficult due to weak the edge profiles generated by a scanning electron beam. Additionally, the tone of the SEM image can be reversed by a charging phenomenon which causes false recognition of lines and spaces to occur in thin film patterns.

This paper addresses high accuracy measurement of thin film...
hardmasks using a new measurement algorithm that is applied to profiles obtained from multiple detectors.

7823-100, Poster Session

**IntenCD and mask-phase uniformity**

I. England, Applied Materials BV (Netherlands); S. Mangan, Y. Cohen, Applied Materials (Israel)

Wafer critical dimension uniformity (CDU) budget for 2x node pose stringent requirements for mask induced errors on wafer level. The 2nm CDU budget regime, consumed partially by across wafer and field process and imaging errors, leave little room for additional mask errors. Amid this restriction, continuous elevated mask influence over the lithographic field, due to higher mask error enhancement factor (MEEF), is imminent and will require special attention.

Traditionally, mask metrology assessments of these errors are based on the divergence of several of the mask process elements into separate evaluations of critical dimension and phase/transmission measurements.

The traditional measurement tools are utilizing different techniques to separately measure each source of non-uniformities and produce the required uniformity maps. Each technique concentrates on a single physical property (e.g., line-width, phase, transmission, etc.) and requires special calibration for the required accuracy, precision and its transformation from mask to the wafer nanometer domain. An alternative to all these measurements was proposed, using IntenCD application in the aerial image of the mask. This application provides a map of mask-induced printed CD variations across the photo-mask.

In this paper we present a study on estimating the mask-induced printed CDU from the aerial image compared to phase and mask-CD measurements. We show that a single aerial IntenCD map can replace a printed CDU from the aerial image compared to phase and mask-CD.

Optimized reticle alignment structures for minimizing aberration sensitivities and pattern shifts

M. A. van de Kerkhof, B. Moest, H. Kok, ASML Netherlands B.V. (Netherlands)

Since the introduction of Blue Align for the 130nm node in 2000, the ASML reticle alignment structures have remained constant. However, with the continued shrink in production structures to 38 nm and below for hyper-NA lithographic tools, we see an opportunity to further optimize these reticle alignment structures to reduce overlay numbers and improve yield.

This opportunity is especially relevant for Dual Patterning applications where pattern shifts under different imaging conditions become critical.

In this paper, we will present a proposal for improved reticle alignment structures to minimize the sensitivities for lens aberrations and thereby to minimize the contribution of reticle alignment to pattern shifts. Some alternatives will also be addressed.

Full compatibility of the proposed alignment structures with older machines as well as continued compatibility of older reticles on the new lithographic tools will be discussed.

Duplicated template for discrete track media

A. Tatsugawa, N. Yamashita, T. Oomatsu, K. Saitou, T. Kato, T. Ishioka, K. Usuki, FUJIFILM Corp. (Japan)

Discrete track recording has been focused for future Hard Disk Drive (HDD) to achieve high recording density. Nanoimprint Lithography (NIL) is the important process for discrete track media since it is possible to transfer the same pattern accurately and repeatedly. NIL template is one of the key component as the master in NIL process, which must have an accurate pattern alignment, an adequate pattern shape for media NIL process, and a large pattern area with uniform line width and height. Furthermore a large number of templates are necessary with the same quality for HDD production.

We have studied the duplication of templates in view of the manufacturability. The pattern is fabricated on a Si wafer by a rotary Electron Beam (EB) writing and Reactive Ion Etching (RIE). The pattern on Si is transferred to a quartz template by UV NIL and RIE with a specially prepared resist [1], and also to a Ni mold by electroplating technique [2].

A whole data area on 2.5-inch hard disk was covered with skewed servo pattern and discrete track with Track Pitch (TP) 70nm, and the pattern on Si master was successfully transferred to a quartz template by the UV-NIL and RIE with a new prepared UV curable material. The cross section of quartz pattern was inspected using Transmission Electron Microscope (TEM), and the tooth width and height were approximately 20nm and 50nm. Also TP60nm quartz template was fabricated without hard mask layers such as chromium on quartz in RIE process with the material. The pattern was formed successfully with 17nm tooth width and 50nm tooth height. It showed high potential for manufacturability of template that it could be made the narrow track for future’s HDD with the simple process, which did not need hard mask deposition and strip. The accuracy of the pattern alignment will be discussed.


Optimize the OPC control recipe with cost function

Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Shanghai Electronic Technology Co. (China)

With the design rule shrinks rapidly, full chip robust Optical Proximity Correction (OPC) will definitely need longer time due to the increasing pattern density. Furthermore, to achieve a perfect OPC control recipe becomes more difficult. For, the critical dimension of the design features is deeply sub-exposure wavelength, and there is only limited room for the OPC correction. Usually very complicated scripts need to be developed to handle the shrinking designs, which can be infinitely complicated. So when you are defining a parameter value in your OPC control recipe, one problem is how to find the optimum setting. And usually there are a bund of parameters in the script, some of which may have impact on others performance. We here demonstrate an approach of how to find the optimized setting of the critical parameters with cost function. And this will be helpful to reduce the difficulty for OPC recipe development.

OPC recipe optimization using simulated annealing

T. S. Desouky, Mentor Graphics Egypt (Egypt)

One of the major problems in the RET flow is OPC recipe creation. The existence of numerous parameters to tune and the interdependence...
between them complicates the process of recipe optimization and makes it very tedious. There is usually no standard methodology to choose the initial values for the recipe settings or to determine stable regions of operation. In fact, parameters are usually optimized independently or chosen to resolve a certain issue for a specific design without quantifying its effect on the quality of the recipe or how it might affect other designs. Another problem arises when a quick fix is needed for an old recipe to build new design masks, and this causes the stacking of many customization statements in the OPC recipe, which in turns increases its complexity. Consequently, the experience of the developer is highly required to build a good as well as a stable recipe. In this context, simulated annealing is proposed to optimize OPC recipes. It will be shown how many parameters can be optimized simultaneously and how we can get insight about the stability of the recipe.

7823-106, Poster Session
Qualification methodology of SRAF insertion at contact holes patterning lithography process
J. Kim, P. J. Lacour, Mentor Graphics Corp. (United States)

Improving process margin of contact holes pattern continues to be one of the critical issues to increase yield in low k1 lithography process. Combination of illumination source optimization and SRAF (Sub-Resolution Assist Feature) has been a common approach to achieve the maximum overall process window. Illumination source optimization and full-chip level SRAF insertion techniques were available by commercial software, which provides the functionalities of model based solution as well as rule base approach. It was proven by the previous studies that such approaches increase overall process window compared with when no SRAF is inserted.

However, there has not been a study to tell if a specific SRAF recipe is actually providing the optimum performance to enlarge the process window, and how much process window improvement can be expected by further recipe tuning efforts. Unspecified manufacturing constraints makes things more complicated to estimate the potential process window improvement. In this study, a quantitative qualification methodology will be introduced regarding how to predict the ideal process window, how to characterize SRAF recipes to tell how much potential process window improvement can be achieved by optimum SRAF insertion setup. SRAF printability considering the mask manufacturing constraints will also be analyzed. In addition, the verification techniques will be discussed about how to classify different sources of patterning hotspots such as correctable hotspots by OPC, SRAF and retarget process. In certain cases, SRAF solution may not exist to meet user’s process window margin specification, named as un-correctable hotspots that cannot be resolved without process/layout change. This situation will also be discussed in this study.

7823-107, Poster Session
CAD for positive line-by-fill SADP process
Q. Li, Mentor Graphics Corp. (United States)

Double patterning (DPT) with ArF water-based immersion systems is emerging to first extend production lithography to $32\text{nm}$ and below. Among different DPT technologies, the two mainstream are LELE and SADP (Self-aligned double patterning). While both LELE and SADP are actively researched and optimized on the process sidecite{DBLP:journals/tcad/BermanKVWZ00}, to more recently proposed new techniques for LELE cite{DBLP:conf/iccad/KahngPXY08}, and to the inherent computational limitation imposed by hierarchy cite{DBLP:journals/tcad/Liu}, CAD support for SADP, on the other hand, is almost non-existent. This lack of CAD support adversely impacts SADP and can override any other concern in SADP’s adoption beyond memory designs.

In this paper, we consider a restricted style of positive line-by-fill SADP process. We will present a general solution that can successfully generate mandrel mask and trim mask for most logic designs, and characteristics of a design manufacturable with this restricted style of positive line-by-fill SADP process.

7823-108, Poster Session
A full-chip MB-SRAF placement for advanced technology nodes using the SRAF guidance map
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Rule-based sub-resolution assist feature (RB-SRAF) has been widely used to improve process marginality in sub-wavelength lithography since 65nm technology node. RB-SRAF worked well with larger pitches and simple designs. RB-SRAF needs long development time with several iterations among litho process engineers, rule-flow developer and design engineers. With the technology shrink, the everlasting design complication has pushed the RB-SRAF to the limit. Starting in 28nm technology node, model-based SRAF (MB-SRAF) placement is needed to achieve required process window (PW) fidelity, especially for the random-logic complex design and semi-dense patterns. The adoption of MB-SRAF is an analogue of the adoption of model-based OPC. MB-SRAF can place needed SRAF where RB-SRAF can not describe. Furthermore, MB-SRAF does not require lengthy rule-flow developments and reduced the need of iterations between process engineers and design engineers. A few papers had proposed using inverse lithography technology (ILT) to place SRAF. Unfortunately, ILT based SRAF placement suffered extremely long running time and additional cost of regularizing the final SRAF to meet mask costs, such as the desire to have simple rectangle shapes.

In this paper, first we describe a realistic production-worthy MB-SRAF technique using the SRAF guidance map, and then we will present the experimental results of SGM full-chip process window against RB-SRAF process window, MRC effects to process window and the full-chip runtime assessments.

The guidance map is an image of the simulation domain, in which each pixel value was derived based on the sensitivity of improving PW on the desired pattern, should that pixel be a SRAF. The higher the value, the better chance SRAF needs to be placed on that pixel. Once the map was constructed, SRAF is extracted based on the value and regulated by the MRC and simple rectangle shapes. For the full-chip placement, SRAF merges among different extraction zones were achieved by evaluating the strength of the signal that improves neighboring PW. After SRAF placement, OPC was applied taking PW into consideration. Realistically, bias or simple OPC might be applied to improve map signal for constructing maps. Figure 1 showed a possible tapeout flow. Figure 2 is an example of guidance map and SRAF. Detail description of this technique will be discussed in the full paper.

This technique has been systematically studied with different sources; different test patterns including through-pitch array, SRAM and random logic; and with differing MRC effects. Figure 3 showed a simple example of placement MRC effect to the PW. The technique has been successfully used in realistic product of 2Xnm technology node. The technique solved the dead-spot created by RB-SRAF and the runtime is compatible to the RB-SRAF. Detail results will be discussed in the full paper.
7823-109, Poster Session

Optical proximity correction challenges with highly elliptical contacts

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The steady march of Moore's law demands ever smaller feature sizes to be printed and Optical Proximity Correction to correct to ever tighter dimensional tolerances. Recently pitch doubling techniques have relieved the pressure on CD reduction, which instead of being achieved lithographically are reduced by subsequent etching or chemical interaction with spin-on layers. CD tolerance reductions, however, still need to match the overall design rule shrinkage. The move to immersion lithography, where effective Numerical Apertures now reach 1.35, has been accompanied by a significantly reduction in depth of focus, especially on isolated contacts. To remedy this, RET techniques such as assist feature placement, have been implemented. Certain local placements of assist features and neighboring contacts are observed to result in highly elliptical contacts being printed. In some layouts small changes in the aspect ratio of the contact on the mask leads to strong changes in the aspect ratio of the printed contact, whereas in other layouts the response is very weak. This effect can be described as an aspect ratio MEEF. The latter type of contact can pose a significant challenge to the OPC recipe which is driven by the need to place the printed contour within a small range of distance from target points placed on the midpoint of edges of a nominally square contact. The OPC challenge naturally will be compounded when the target layout is rectangular in the opposite sense to the natural elliptical shape of the printed contact. Approaches to solving this can vary from intervening at the assist feature placement stage, at the possible loss of depth of focus, to accepting a certain degree of ellipticity in the final contour and making the OPC recipe concentrate on minimizing any residual errors. This paper investigates which contact layouts are most challenging, discusses the compromises associated with achieving the correction target and results are shown from a few different approaches to resolving these issues.

7823-110, Poster Session

Manufacturing cost reduction and extending scanner life by using inverse lithography technology with assist feature

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Patterning of contact holes using KrF lithography system is one of the most challenging tasks for the sub-90nm technology node, Contact hole patterns can be printed with a KrF lithography system using Off-Axis Illumination (OAI) such as Quasar or Quadrupole. However, such a source usually offers poor image contrast and poor depth of focus (DOF), especially for isolated contact holes. In addition to image contrast and DOF, circularity of hole shape is also an important parameter for device performance. Sub-resolution assist features (SRAF) can be used to improve the image contrast, DOF and circularity for isolated contact holes. Application of SRAFs, modifies the intensity profile of isolated features to be more like dense ones, improving the focal response of the isolated feature. The insertion of SRAFs in a contact design is most commonly done using rule-based scripting, where the initial rules for configuring the SRAFs are derived using a simulation tool to determine the distance of assist features to main feature, and the size and number of assist features to be used. However in the case of random contact holes, rule-based SRAF placement is a nearly impossible task.

To address this problem, an inverse lithography technique was successfully used to treat random contact holes. The impact of SRAF configuration on pattern profile, especially circularity and process margin, is demonstrated. It is also shown that the experimental data are easily predicted by calibrated aerial image simulation results. Finally, a methodology for optimizing SRAF rules using inverse lithography technology is described. Results to be shared are PW comparison of full chip between POR & ILT, manufacturing costs between POR & ILT, chip yield between POR & ILT, and scanner life extension studies.

7823-111, Poster Session

Affordable and process window increasing novel mask-writing technique

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When optimizing for a factor, such as process window, more complex mask patterns are often necessary to achieve the desired depth of focus. Complex mask patterns require more shots when written with VSB systems, increasing the component of mask cost associated with writing time. For this reason, we desire to determine the mask patterns that meet necessary lithographic manufacturing objectives. Luminescent ILT provides means to constrain complexity of mask solutions, each of which is optimized to meet lithographic objectives within the bounds of the constraints. This paper, using NSC fracturing techniques that enable to convert traditional semiconductor mask design data to manufacturing data for mask writer with less shots, details ILT mask simplification schemes (yet, maintaining required process window) on contact arrays and random logic. Ultimately this method enables litho and mask engineers balance lithographic requirements with mask manufacturing complexity and related cost. Results presented in this paper will show reduction in shot counts of masks that meet customer PW requirements.

7823-112, Poster Session

Substrate aware OPC rules for block levels generated using physical resist simulation

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Implant level photolithography processes are becoming more and more challenging due to ever-decreasing CD requirements while still need meet cost/simplicity control. Optical Proximity Correction (OPC) using models created based on data from plain silicon substrate is having difficulties to accommodate the various real device/design scenarios. In this paper, by simulation using well calibrated physical resist model, we present substrate aware OPC rules to account for effects from substrate, such as material change, geometry variation etc, that are impossible to simulate in an empirical OPC model. Wafer data comparison/verification is also discussed.

7823-113, Poster Session

Multiple models versus single compromise model for doped-poly, double-patterning OPC

L. S. Melvin III, J. Li, Synopsys, Inc. (United States); E. Vidal-Russell, Micron Technology, Inc. (United States)

As a final step before mask tapeout for semiconductor fabrication, proximity and manufacturing correction (OPC) are typically performed using a single process model which predicts proximity error effects for every polygon on a 2D layout. This paper examines two applications
of current interest, the etching of n and p-type doped poly and an example of double patterning (DPT), in which measured CD data falls into two populations not easily fit by a single model. In both cases the proximity behavior of the layer to be corrected is influenced by a previous masking step. Thus a multiple model approach, in which different OPC models are applied to different parts of the layout as identified by the previous masking step, may yield improvements over the standard approach. In this paper the performance of a single “compromise” model vs. multiple models is compared for doped poly etch and DPT. Relative model performance is gauged based on calibration, correction and verification results on various layout geometries.

7823-114, Poster Session

High-pattern-fidelity inverse mask design incorporating an innovative image-contrast optimization algorithm

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Semiconductor fabrication is the cornerstone of the current IC (Integrated Circuit) industry. With advances in microlithography now pushing towards nano-scale features, the problem of how to print circuit layouts on wafers has become more intricate and convoluted. Optical Proximity Correction (OPC) is a resolution enhancement technique that modifies mask layout designs in order to minimize their distortion when transferred to silicon. A good OPC implementation may prove sufficient for a given process technology, precluding the need for a more expensive alternative, like Double Patterning, Alternating Phase Shift Mask (AltPSM), Immersion Lithography and so on. Evidently, OPC has clear advantages in efficiency and manufacturing cost.

Segment-based OPC has been the general industry approach and has proven successful through many CMOS generations. Because it only modifies existing edges in the layout, segment-based OPC has the advantage of being easy to implement, particularly in iterative algorithms. However, as the Critical Dimension (CD) becomes ever smaller, this type edge-only compensation is not expressive enough to exploit the full range of possible mask corrections. Therefore, the inverse mask design, or named Inverse Lithography Technology (ILT) that optimizes the cost function, has been proposed as an alternative due to its more relaxed constraints and full-mask approach. However, the cost function is usually employed to evaluate the resist image and aerial image in the most of current studies. Such treatments are less aware of the image contrast which is definitely important in optical microlithography. Besides, inverse calculation is faced with several problems, including bad convergence and the existence of local minima. To get rid of these issues, many approaches have been proposed, like pixel-flipping, shape-based, gradient strategies and so on. Still, the inversion approaches needs to be further developed to become the next-generation OPC.

There are two contributions in this paper. First, we propose an image contrast evaluation cost function and derive its’ formulation for image gradient descent optimization. Because the contrast is a first order differential operation, such cost function is sensitive on aerial image variations which usually occur at the pattern edges. Second, we develop an image-gradient-based algorithm to simultaneously optimize various cost functions for inverse mask design. The algorithm employs an iterative approach which evaluates the gradient decent of objective functions including (1) the resist image, (2) aerial image, and (3) the aerial image contrast with a pre-assigned step length. Three different coefficients are respectively assigned to the cost functions to emphasize the degree of importance.

7823-115, Poster Session

Simultaneous source-mask optimization: a numerical combining method

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A new method for combined Source-Mask Optimization (SMO) is presented.

In order to produce optimum imaging fidelity with respect to either exposure latitude, depth of defocus or other metrics like minimum MEEF or maximum contrast the presented method aims to leverage both, the available degrees of freedom of a pixelated source and those available for the mask layout. The approach described in this paper is designed as to work with dissected mask polygons. The dissection of the mask patterns is to be performed in advance (before SMO) with the Synopsys Proteus engine, providing the available degrees of freedom for mask pattern optimization.

This is similar to mask optimization as done in optical proximity correction (OPC). Additionally, however, the illumination source will be simultaneously optimized. The presented SMO approach borrows many of the performance enhancement methods of OPC software for mask correction, but is especially designed as to simultaneously optimize a pixelated source shape as nowadays available in a production environment. Designed as a numerical optimization approach the presented SMO method is able to assess in acceptable times several hundred thousand source-mask combinations for a small (but critical) layout snippet of a few square microns.

This allows a global optimization scheme to be applied to the SMO problem which is expected to better explore the optimization space and thus to yield an improved solution quality. In this paper the simultaneous source-mask optimization method is applied to an example and the results are compared to sequential co-optimization approaches where source and mask are optimized separately.

7823-149, Poster Session

Optimization of double patterning split by analyzing the diffraction orders in the pupil plane

N. Zeggagoui, F. Farys, Y. Trouiller, E. Yesilada, F. Robert, STMicroelectronics (France)

In double patterning technology (DPT), two adjacent features must be assigned opposite colors corresponding to different exposures if their pitch is less than a predefined minimum coloring pitch. However, certain design orientations for which pattern features separated by more than the minimum coloring pitch cannot be imaged with either of the two exposures. In such cases, there are no aerial images formed because in these directions there are no constructive interferences between diffractive orders in the pupil plane. The 22nm and 16nm nodes will require the use of pixelized sources that will be generated using SMO (source mask co-optimization). Such pixelized sources while helpful in improving the contrast for certain configurations will lead to degrade contrast for other configurations compared to non pixelized sources. Therefore, we analyze the diffractive orders interactions in the pupil plane in order to detect forbidden orientations in the design and thus propose a decomposition to overcome the problem.
The CD uniformity improvement for ArF extension using mask DFM (design for manufacturing)

B. M. Nam, Y. Lee, S. Oh, Y. Kim, M. Kim, C. Choi, T. Ha, C. Kim, Hynix Semiconductor Inc. (Korea, Republic of)

With decreasing feature size, the requirements related to patterning of photomasks have become crucial for achieving the required yield of wafer fab. With conventional E-beam lithography and reactive ion etching platforms, significant proximity dependent nonlinearity of mask features sizes ranged from micro-meters to less than 100 nano-meters, can no longer be compensated accurately by traditional means of process controls, E-beam proximity correction. Advanced mask patterning technique is thus required to compensate mask local patterning effects due from E-beam lithography (litho) to reactive ion etching (etch) process steps.

In this study, we introduce the mask dummy scheme from both 1-dimensional (L/S) & 2-dimensional (hole) block edge CD uniformity data. We performed the experimental analysis for the CD uniformity both mask & wafer by mask dummy effects.

EUV-mask defect mitigation through pattern placement

M. Abbas, J. M. Burns, Synopsys, Inc. (United States); Y. A. Liu, P. Yan, Intel Corp. (United States)

One of the challenges of EUVL is to bring EUV mask blank defect levels to zero. With uncertainty on when defect free masks may be routinely available, we explore a possibility for effectively using defective EUV mask blanks in production with a defect avoidance strategy. The key idea is to position the pattern/layout on the blank where the defects do not impact the final wafer image. Assuming that layout designs contain some non-critical areas in which defects can be safely positioned, it may be possible to align these regions with a given, small set of defect positions mapped from an imperfect mask blank.

Using a few representative assortment of current-node, full-chip layout patterns we run multiple trials against real blank defect maps with various defect counts successfully. Our goal is to assess the probabilities that defect avoidance will work as a function of mask blank defect count, and by lithography layer.

Integrated mask and optics simulations for corner rounding effect in OPC modeling

J. Xue, Z. Deng, Synopsys, Inc. (United States); K. Koo, Synopsys Korea Inc. (Korea, Republic of); Y. Zhang, Y. Fan, J. P. Shiely, Synopsys, Inc. (United States); T. Schmoeller, Synopsys GmbH (Germany); S. Lee, Synopsys Korea Inc. (Korea, Republic of)

The quality of the photolithographic pattern transfer depends on the exposure process and on the mask pattern fidelity. As device feature sizes shrink to 45nm and beyond, the impact of mask shape distortion due to the mask writing process is no longer negligible, and mask corner rounding (MCR) becomes an important component of CD error budgets in optical proximity correction (OPC) modeling and related applications. In this paper, we analyze the MCR effects to the aerial image and to the resist image in OPC modeling, and introduce a novel MCR modeling approach based on Synopsys’ Integrated Mask and Optics (IMO) modeling framework. A convolution between a two-dimensional kernel and the ideal mask layout is used to approximate the actual mask pattern. The various point spread functions and a weighted kernel selection scheme are applied on the ideal mask layout. The mask contour analysis indicates good continuity and fidelity of simulated mask patterns. The MCR function is integrated with the OPC calibration process. This MCR integrated approach achieves significant improvements in modeling 2D patterns, such as line end and contact structures. The results show that the integrated MCR simulation technique is very promising and likely necessary for full-chip OPC modeling for the advanced technology nodes and upcoming generations.
Design for e-beam: design insights for direct-write maskless lithography

A. Fujimura, D2S, Inc. (United States)

Designers always want maximum freedom in design, but they understand that chips have to yield and at a reasonable cost. The strong ecosystem support of restricted design rules to make 193i workable for sub-30nm nodes is evidence of this. In direct write e-beam, there are design insights that lead to a tangible improvement in throughput while minimizing the restrictions on the designert. It turns out that a smaller number of primitive cells in a standard cell methodology can enable data compression for multi-beam systems, and enable faster write times for character projection in VSB-based multiple column machines. This requires a co-design of the standard cell library with the stencil mask (either virtual or real) that goes into the machine. This co-design step is required only once per library and not on a design-by-design basis, thus minimizing the impact on designers. 10-20X speedups in e-beam throughput depending on layer are seen in typical layout examples for character projection machines.

ML2 in SMT

S. Wurm, SEMATECH North (United States)

No abstract available

ML2 versus EUV

S. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

No abstract available

Pattern verification for the sub-20-nm era

I. Holcman, Applied Materials (Israel)

The industry has converged on EUV lithography as the most promising candidate to replace ArF for the 22nm half-pitch node and beyond. Alternatively, ML2 is being pursued as a more cost-effective solution, especially for smaller wafer volumes and prototyping.

Both technologies have their individual approaches and problems when it comes to mask and wafer inspection. ML2 however has the added complexity, that the ultimate pattern verification step, patterned mask inspection in D:Db mode is not possible.

A new approach and flow is needed.

A promising candidate is Electron Beam based Wafer Inspection. While it certainly has the resolution, and is a long proven technology, throughput is in general considered an issue.

In this talk we will summarize the studies and present results of developing solutions to EB based Wafer and Mask Inspection. We will take a special look at the requirements for pattern verification, the resolution and throughput needs, and the technological answers to these challenges. We will investigate the options for EB2M applications, and the sensitivities that can be achieved. The various configuration options for multi-beam approaches will be discussed.

In a final assessment we will look at the economics of MBEBI for wafer and masks, and the possible transparency of these inspections in both EUV and ML2.

Geometrically induced dose correction method for e-beam lithography applications

R. R. Galler, EQUIcon Software GmbH Jena (Germany); K. Choi, M. S. Gutsch, C. K. Hohle, Fraunhofer-Ctr. Nanoelektronische Technologien (Germany); M. Krueger, EQUIcon Software GmbH Jena (Germany); L. Ramos, Vistec Electron Beam GmbH (Germany); M. Suelzle, EQUIcon Software GmbH Jena (Germany); U. Weidenmueller, Vistec Electron Beam GmbH (Germany)

The e-beam lithography is faced with increasing challenges to achieve a satisfying patterning of structures with critical dimensions of about 32 nm or below, especially if a technological process with production relevance is used. The reason for this issue is the physical characteristic of the whole transfer process used to print a resist profile onto the exposed substrate. The final resist profile differs from the dose distribution of the exposed e-beam shot which is often different from the desired shape itself. That all leads to an unavoidable blurring of the deposited e-beam energy around the desired shape and is usually described by a so called process proximity function (PPF) that is approximated by a superposition of two or more Gaussian functions.

The PPF includes the e-beam blur, electron forward scattering and resist effects (often described altogether by the so called alpha-parameter of the PPF) as well as the backscattering effect (often described by the so called beta-parameter of the PPF). For these physical reasons, when the desired critical dimension of a structure is near or below the alpha-parameter of the PPF, depending on its environment it may be just impossible to print the structure because of the vanishing image contrast.

In previous papers [1, 2, 3] we have shown by means of the simulation feature of the ePLACE data prep package that in this situation only a modification of both the geometry and the dose assignment of the shapes can preserve the printability of critical structures and how this is done by the geometrical induced dose correction method implemented in ePLACE. The simulation results for test structures are now validated by experimental data for test and real structures showing the advantage of the new method.

In this paper we will publish the results of the related exposures - done on a Vistec SB3050DW shaped e-beam writer - of test and real patterns demonstrating the practical importance of the geometrical induced dose correction method for layouts with CD's of 32 nm and below.

3. R. Galler et al, “Modified Dose Correction Strategy for better Pattern Contrast”, EMLC 2010
REBL (Reflective Electron Beam Lithography) is a program for the development of a novel approach for high-throughput maskless lithography. The program at KLA-Tencor is funded under the DARPA Maskless Nanowriter Program. A DPG (digital pattern generator) chip containing 1 million reflective pixels that can be turned on or off is used to project a pattern onto the wafer. The DARPA program is targeting a throughput of 5 to 7 wafers per hour at the 45 nm node, and we will describe extensions to both increase the throughput as well as extend the system to the 32 nm node and beyond.

REBL utilizes several novel technologies to generate and expose lithographic patterns at throughputs that could make ebeam maskless lithography feasible for manufacturing. The DPG will incorporate CMOS on-chip circuitry in order to provide the extremely high data rates without excessive interconnect. The exposure strategy uses a TDI (time delay integration) technique of scrolling data across the DPG in synchronicity with the stage motion, which provides both redundancy for defective pixels as well as inter-pixel exposure control for proximity effect correction and sub-pixel edge placement. The stage will be a rotary mag-lev design that can hold and expose up to 6 wafers at a time. Wafer registration will be based on non-actinic optical metrology of marks placed on the wafers as well as on spokes between wafers.

In this paper we will give an overview of the REBL program and also an update on the latest progress. Recent results from our DPG test chips along with corresponding resist prints will be shown. In order to optimize the pixel contrast and prevent cross-talk between neighboring pixels, a microlens structure is built on top of each pixel using CMOS fabrication technology. We will also discuss our new column design which uses a Wien filter that enables a smaller column and also has better performance over the previous prism-based column.

Multishaped-beam (MSB): an evolutionary approach for high-throughput e-beam lithography

M. Slodowski, H. Doering, I. A. Stolberg, W. H. Dorf, Vistec Electron Beam GmbH (Germany)

The development of next-generation lithography (NGL) such as EUV, nanoimprint lithography and maskless lithography (ML2) are driven by the half pitch reduction and increasing integration density of integrated circuits down to the 22nm node and beyond. For electron beam direct write (EBDW) several revolutionary pixel based concepts are under development since several years. By contrast an evolutionary and full package high throughput multi electron-beam approach called Multi Shaped Beam (MSB), which is based on proven Variable Shaped Beam (VSB) technology, will be presented in this paper.

In the recent decade VSB has already been applied in EBDW for device learning, early prototyping and low volume fabrication in production environments. Above all the high resolution and the high flexibility due to the prevention of masks made it an attractive solution for advanced technology nodes down to 32nm half pitch. The limitation in throughput of VSB has been mitigated in a major extension of VSB by the qualification of the cell projection (CP) technology concurrently used with VSB. With CP more pixels in complex shapes can be projected in one shot, enabling an essential shot count reduction.

The most advanced step to extend the mature VSB technology for higher throughput is its parallelization in one column applying MEMS based multi deflection arrays. With this Vistec MSB technology, multiple shaped beamlets are generated simultaneously, each controllable individually in shape size and beam on time. Compared to pixel based ML2 approaches the MSB technology enables the maskless, variable and parallel projection of a number of pixels per beamlet times the number of beamlets.

Basic concepts, exposure examples and performance results of each of the described throughput enhancement steps will be presented. Finally, the paper will give an outlook on the MSB product roadmap.

High-throughput maskless lithography

B. J. Kampherbeek, MAPPER Lithography (Netherlands)

No abstract available

A lifetime study of EUV masks

E. E. Gallagher, U. Okoroanyanwu, O. R. Wood II, L. M. Kindt, M. J. Barrett, IBM Corp. (United States); H. Kato, Toshiba America Electronic Components, Inc. (United States); G. Landie, STMicroelectronics (United States)

Extreme Ultraviolet Lithography (EUVL) offers the promise of dramatically improved resolution at the price of introducing a complex web of new lithographic challenges. The most conspicuous departure from DUV lithography is that exposure wavelength is reduced from 193 to 13.5nm. Under exposure at this short EUV wavelength, all materials absorb. Consequently the scanner optics and masks must be reflective and wafer exposure occurs in vacuum without a pellicle to protect the mask. This represents a dramatic shift from the current DUV mask use case. For example, the mask will have to be cleaned after exposure to remove contamination accumulated instead of being protected for its lifetime by a transparent pellicle. The impact of cycling through the exposure tool and being cleaned multiple times will be
studied using particle inspection, scatterometry, reflectometry and AFM measurements. The results will be used to identify contamination modes and to propose best practices for EUVL mask exposure.

7823-40, Session 10
The control of EUV-mask defects on mask making process
K. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)
A successful extreme ultraviolet lithography (EUVL) requires high quality EUV mask blanks that should be controlled to defect free. Moreover, EUV mask blanks must have zero defects down to 30 nm diameter sizes. The concerns of EUV mask defects are including defects present on the substrate, adding during the multilayer (ML) deposition process (phase defect), adding by handling the mask blank, and producing during mask making process. Excepting the defects from mask blank making, the etching process is one of important concern for defects production. In this paper, the productions of defect were focused on etching process for EUV mask making defect control. The etching by-product by absorber patterning can be the main source of defect production. By controlling the chamber season, gas flow, and source/bias power, the etching recipes are optimized for reducing defects and well pattern profiles. Five etching recipes were applied for three different absorber materials, including Ta-base and Si-base, by design of experiment (DOE) to investigate the defect production from etching process. The defect types are related with various causes, by optimizing the conditions of etching recipe, the different types of defect are effectively controlled for EUV mask process. The defects from mask making process were inspected by KLA6XX. According to the inspection results, the optimized etching recipes provide the way to reduce the defects larger than 30 nm for etch absorber materials of EUV mask making.

7823-41, Session 10
Impact of mask topography and multilayer stack on high-NA imaging of EUV masks
J. Ruoff, Carl Zeiss SMT AG (Germany)
EUV reticles differ in many aspects from optical transmission reticles for DUV or VUV. Due to the non-existence of transparent materials in the EUV regime, the mask has to be used in reflection mode which is realized by putting the patterned absorber material onto a dielectric mirror, consisting of 40 or more bilayers of materials with alternating higher and lower refractive index. Moreover, the reticle has to be obliquely illuminated since otherwise the light would be reflected back into the illuminator. It is well known that this oblique illumination leads to a shadowing effect, which in turn is responsible for the fact that horizontal and vertical lines with the same width on reticle will have different CDs on wafer side. Moreover, for EUV the illumination is not telecentric on the reticle side, which leads to a rather tight mask focus control, since a defocusing of the mask would lead to an undesired pattern shift. With EUV being the most promising candidate for future lithographic nodes, the requirement for continuous shrink can be satisfied pretty much along the same route that has been successfully taken by optical lithography, i.e. by increasing the NA and reducing k1. From optical lithography we know that only for hyper NA reticles the deviations from the Kirchhoff approach started to become non-negligible and rigorous mask computations are necessary in order to correctly taking into account the polarization effects. Typical 3D effects for optical transmission masks are polarization dependent diffraction efficiencies and polarization induced astigmatism, which lead to different focus shifts for horizontal and vertical lines [1]. For EUV reticles, the absorber thickness is several times the wavelength, and the deviations from the Kirchhoff mask approach are already non-negligible at NA = 0.25, and manifest themselves e.g. in the well-known shadowing effect. For the current EUV scanners the shadowing induced HV differences still can be compensated by rather simple OPC on the reticle. However, for increasing NA and shrinking feature sizes aberration-like effects start to occur, growing rather fast. It has been shown that these electromagnetic effects can cause imaging aberrations, which can be described by the well-known Zernike polynomials. For instance, astigmatic aberrations, which lead to focus splits for horizontal and vertical lines, and spherical aberrations, which induce process window tilts, will have non-negligible impact on imaging [2]. From purely optical design considerations there is no fundamental obstacle to increase the NA up to 0.7 or even beyond. With the current reticle layout, it is possible to obtain satisfactory imaging results up to NA = 0.32, however, for larger NA the aerial images strongly degrade. This is mainly due to the fact that with increasing NA the chief ray tilting angle has to grow as well, which means that shadowing and non-telecentricity effects become much more severe. Moreover, the current multilayer designs do not support the growing incidence angle range on the reticle. It is therefore of utmost importance to gain a thorough understanding of the electromagnetic mask effects, which have to be taken into account when designing reticles for high NA projection lenses due to the strong increase of the above mentioned image deteriorating consequences. We will examine in detail the influence of the multilayer and the effects of the finite absorber height on the imaging with high NA optics and devise measures which have to be taken into consideration when pushing the NA beyond the current values.

References:

7823-42, Session 10
EUV-mask stack optimization for enhanced-imaging performance
E. Van Setten, ASML Netherlands B.V. (Netherlands); M. V. Dusa, ASM Belgium N.V. (Belgium); R. de Kruif, N. Davydova, K. Feenstra, C. Wagner, ASML Netherlands B.V. (Netherlands); P. Spies, T. Bret, M. Waiblinger, Carl Zeiss SMS GmbH (Germany)
EUVL requires the use of reflective optics including a reflective mask. The reticle blank contains a reflecting multilayer, tuned for 13.5nm, and an absorber which defines the dark areas. The EUV mask is a complex optical element with many more parameters than the CD uniformity of the patterned features that impact the final wafer CDU. Peak reflectivity, centroid wavelength and absorber stack height variations need to be tightly controlled for optimum performance. Furthermore the oblique incidence of light in combination with the small wavelength compared to the mask topography causes a number of effects which are unique to EUV, such as an H-V CD offset and an orientation dependent pattern placement error. These so-called shadowing effects can be corrected by means of OPC, but also need to be considered in the mask stack design.
In this paper we will show that it is possible to improve the imaging performance significantly by reducing the sensitivity to mask making variations such as capping layer thickness, centroid wavelength and absorber stack height variations. The impact of absorber stack height variations on CD and placement will be determined experimentally by changing the local absorber stack height using the novel e-beam based reticle repair tool MeRiT® HR 32 from Carl Zeiss in combination with exposures on ASML’s alpha demo tool. The impact of absorber reflectivity will be shown to derive requirements for the reticle border around the image field, as well as the impact of phase errors on Bossung tilt. Features down to 24nm half pitch from several device layers, such as NAND-Flash and SRAM layers, will be evaluated.
for multiple masks, comparing process windows and CD uniformity from exposures on ASML’s alpha demo tool and the NXE:3100 preproduction tool. The outcome may serve as guidance for EUV mask manufacturing to support the introduction of EUV for HVM.

7823-43, Session 10

Assessing pattern inspection solutions for EUVL reticles at the 11-nm logic node

T. Liang, J. F. Magana, F. A. Ghadiali, G. Zhang, Intel Corp. (United States)

With the complementary use of wafer print and laboratory tools, the basic tool set and procedures exist today for extreme ultraviolet lithography (EUVL) multilayer blank and reticle defect characterization and process development, but they are not adequate for technology development or for pilotline production. To enable the fabrication of defect-free reticles for EUVL production, the industry is assessing and developing solutions for three critical tools: multilayer blank inspection, pattern inspection and aerial image measurement (AIM) for defect disposition. Unlike blank inspection and AIM tools, the tool requirements and capability for pattern inspection are much more challenging to evaluate because one must consider the dependency of inspection sensitivity on the type of device patterns and the location of defects. While data have shown that DUV optical and electron beam based tools are expected to meet the requirements for 16nm logic node, substantial capability gaps exist for the 11nm logic node.

In this paper, we report our evaluation of the capability of 193nm optical and e-beam inspection tools for different pattern layers of 11nm node generic design rules. A set of programmed defect test reticles are fabricated with different absorber stacks and inspected on multiple tools. Inspection sensitivity is measured at different illumination and polarization conditions to determine the optimal configuration for each pattern layer. We also quantify the capability gaps and discuss the required tool development to close these gaps in order to meet both the sensitivity and timing needs for EUVL insertion into production.

7823-44, Session 10

EUV-mask inspection technologies for contact (hole) layers for 2-nm hp and beyond

G. A. Inderhees, D. C. Wack, T. Fu, Q. Zhang, Y. Xiong, KLA-Tencor Corp. (United States)

Reticle quality and the capability to qualify a reticle are key issues for EUV Lithography.

We expect current and planned optical inspection systems will provide inspection capability adequate for development and production of 2X hp masks. We illustrate inspection technology extendibility through simulation of 193 nm-based inspection of advanced EUV patterned masks.

Building upon work that we published at the SPIE Advanced Lithography Conference in Feb 2010 [1], we show simulation results for defect sensitivity and contrast on contact layers with various 1D and 2D programmed defects. We explore the influence of EUV absorber design for 193 nm optical inspection, and show the impact of off-axis illumination and advanced polarization techniques on inspector performance. We will discuss the trade-offs and issues required to support two absorber stacks, one optimized for line/space layers, and one optimized for contact-type designs.


7823-45, Session 11

Investigation of carbon contamination growth dependency on Ruthenium surface property of EUV mask


Carbon contamination for EUV mask is known to be created by subsequent processes as following. First, hydrocarbons in environment are adsorbed on Capping layer surface. The adsorbed hydrocarbons are cracked by EUV light and secondary electrons bounced from Capping layer on Multilayer. Finally, those cracked molecules of Carbon, Hydrogen, or their compounds are re-adsorbed on the Capping layer with being packed into a dense amorphous carbon film, resulting in severe Reflectivity drop.

It has been tried to mitigate Carbon contamination on EUV mask surface by means of changing Capping layer materials. Meanwhile, it is very difficult to find the best material for Capping layer to meet every specification for mask fabrication process and performance. The most preferred direction without any material change was to control the exposure environment inside scanner while scanner environmental control could be limited by cost and effectiveness.

Based on proposed mechanism for Carbon contamination on EUV mask, the initial adsorption of hydrocarbons on Capping layer surface seems to be very important step for Carbon contamination buildup and final reflectivity drop on EUV mask. There has been little research on whether Carbon contamination growth would be affected by different degree of adsorption of hydrocarbon on Capping layer surface.

In this paper, we will investigate whether various degree of hydrocarbon adsorption could lead to different growth characteristics of Carbon contamination on EUV mask. We are also going to investigate any feasible and efficient methodologies to render different degree of hydrocarbon adsorption to mask surface. If surface conditioning processes could create various degrees of hydrocarbon adsorption and finally Carbon contamination buildup, they can play a pivotal role in the control of Carbon contamination and Reflectivity for EUV mask.

7823-46, Session 11

Current status and challenges in EUV reticle defect detection: a case study of using a real product

J. F. Magana, M. Chandhok, T. F. Crimmins, F. A. Ghadiali, T. Liang, G. Zhang, Intel Corp. (United States)

One of the key capabilities which must be in place before EUV lithography is implemented in high volume manufacturing is tooling for rapid and reliable detection of reticle defects. Reticle defects arise from a multitude of sources: substrate polishing and cleaning, multilayer and absorber thin films deposition, patterning, shipping and handling, etc.. A critical element of the EUV mask infrastructure is tooling for detection and categorization of reticle defects from these various sources so that these defects can be eliminated, repaired or mitigated. While it is widely agreed that ultimately this tooling will include actinic inspection, availability of AIMS tooling is realistically at least several years away. The current work is a case study describing the detection of reticle defects without the use of AIMS. This study makes use of commercially available blank material and a real product pattern. Aim of this study is not to benchmark the best or “champion” EUV mask defect density achievable today. Rather, the objective of this work is to examine the status, challenges and gaps commonly encountered in the current inspection capabilities from blank production to wafer printing.
Natural EUV-mask blank defects: evidence, timely detection, analysis, and outlook


Nowadays mask defectivity is considered as the most important challenge to prepare EUV lithography in time for use in high volume manufacturing of the 22nm half-pitch device node and below. Especially the EUV specific multi-layer (ML) type defects are a potential threat, as they are not readily repaired. We earlier reported [1] on the detection of printing defects that were considered ML-type defects, where both the blank inspection and mask inspection used were not sensitive enough to detect them. We use wafer defect inspection followed by repeater analysis, followed by wafer review and mask review. Unique in our work is that we focus on natural defects and on the insight in how far dedicated blank- (and mask-) inspection tools detected them. This important learning helps to inspire initiatives in the EUVL community to mitigate the mask defectivity issue, such as the EUV Mask Infrastructure Working Group of Sematech. Over the last two years of experience with the world’s first full-field EUV scanner, the ASML Alpha Demo Tool (ADT), several EUV reticles with an optimized layout for defectivity testing have been obtained from multiple suppliers. A combination of blank-, mask- and wafer inspection is used to monitor the progress made by blank and mask vendors in reducing defect density on mask. The present best result will be compared to the target that the industry has defined for mask defect density.

In parallel, major effort has been put in the investigation of the challenges that metrology tools are facing in finding all printing defects on an EUV mask. Backward correlation of the printing defects to blank inspection (and mask inspection) can visualize the gaps that such tools have in detecting the EUV specific ML defects. Atomic Force Microscopy (AFM) analysis of defects found only by wafer inspection has proven the presence of a few-nm high ML-defects that the blank inspection tool used had missed. Meanwhile a multitude of newer tools with blank inspection capability have become available. Recent work continues to target for a full picture of the capabilities of all available tools. Those are being benchmarked versus the needs dictated by the analysis of the printing behavior of natural defects.

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Printability of EUVL mask defect detected by actinic blanks inspection tool and 199-nm pattern inspection tool


Extreme Ultraviolet Lithography (EUVL) is one of the most promising technologies in lithography for the fabrication of ULSI devices with 22nm half-pitch (HP) and beyond. Mask plays a key role in EUVL, and should be regarded as an integral part of a lithographic system. EUV mask is required to exhibit high lithographic performance, such as higher image contrast, smaller shadowing effect caused by oblique illumination, low thermal expansion of substrate material, better flatness control, etc. Our earlier work on the improvement of lithographic performance of EUV mask had demonstrated that by a thinning down of LR-TaBN absorber with EUV light-shield area, the shadowing effect could be reduced without any loss in printability. On the other hand, one of the key challenges before EUVL is to make defect-free masks. There are three main categories of mask defects: phase defects embedded within the multilayer blank, absorber defects formed during the patterning of absorber, and particles resulting from mask handling. It is important to identify the root cause of defects in order to realize defect-free masks and it is also necessary to set suitable specifications of mask defects for the production of ULSI devices.

In this paper, we evaluate printability of mask blank defects and mask pattern defects exposed by full-field scanner EUV1, using with a world first full-field, actinic blank inspection tool and a new EUV mask inspection tool with 199 nm wavelength DUV light. And based on a series of results, we discuss the critical defect specification of 32nm HP and beyond.

This work was supported by New Energy and Industrial Technology Development Organization (NEDO).

Improvement of actinic blank inspection and phase defect analysis

T. Yamane, T. Tanaka, T. Terasawa, O. Suga, Semiconductor Leading Edge Technologies, Inc. (Japan)

Extreme Ultraviolet Lithography (EUVL) is a promising technology for ULSI devices with a half pitch of 32 nm and below. However, the fabrication of defect-free mask blanks and their inspection continue to be a matter of concern for the implementation of EUV. A multilayer phase defect is initiated by some kind of disorder in the multilayer that is generated during the multilayer film growth if a particle or a pit happens to reside on a quartz substrate surface. Because this kind of defect is hardly noticeable on the mask blank surface with a conventional inspection system, an actinic (at wavelength) defect inspection technique is being pursued.

To address this issue we have developed an actinic full-field EUVL mask blank inspection system to detect multilayer phase defect by employing a dark field imaging technique. Based on our estimation of impact of a phase defect on a wafer for 22 and 32 nm HP devices, we maintain that our target of inspection sensitivity was to capture a phase defect caused by a 1.5 nm-high and 40 nm-wide protrusion on a multilayer surface. In this system, the light scattered from a mask blank surface reaches a CCD camera where a defect is captured as a spot signal brighter than a pre-determined threshold. A lower threshold increases the defect sensitivity but it also results in false defect detection, primarily due to CCD readout noise. To address this issue, replacement of illumination parts, improvement of auto-focus accuracy, and application of noise filtering algorithm were performed. Then, detection probability of a 1.5 nm-high and 60 nm-wide defect was improved to nearly 100 % with no false defects. On the other hand, although our target of the inspection time for full field of a mask blank was 2 hours, the actual inspection time was 14.5 hours. For improvement of the throughput, a new CCD camera was installed onto the system. The new CCD camera enables bi-directional scanning for inspection and then shortens the return trip to the next row as compared with one direction scanning inspection. It also decreases the noise signal intensity and then enables a faster scanning speed without sacrificing defect detection sensitivity.

In this presentation, the current defect sensitivity will be reported, and improvement of throughput will be demonstrated. The inspection result of several mask blanks will be shown, and the analysis result of phase defects that impact on 22 nm HP devices and below will be presented.

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Conference 7823: Photomask Technology

7823-142, Session 11
Investigation of the influence of resist patterning on absorber LWR for 22-nm-node EUV lithography
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Achieving the specifications of resolution, sensitivity and line width roughness (LWR) of wafer resist is one of the top challenges of bringing extreme ultraviolet lithography (EUVL) into high volume manufacturing. Contributions to the resist LWR can be divided into two categories, chemical properties of the resist and aerial image. Chemical properties of the resist are complicated and many factors contribute to LWR, such as polymer size, sensitivity, surface reaction etc. Aerial image LWR is much simply determined by the optical properties of a mask and a scanner. Since very small LWR value of the resist is needed, EUV mask LWR is also set very severely from ITRS [1].

In our previous work [2], we fixed parameters of LWR measurement for future development work and reported current LWR value is hard to reach the target one at 22nm node set by ITRS. Comparing mask resist LWR and absorber LWR, absorber LWR almost depends on resist patterning, so development of mask resist material and patterning process should be accelerated.

In this paper, we will present the results of characteristic analysis of EUV mask LWR using many samples and various processes. We will also classify the factor of LWR using the power spectral density (PSD) analysis.

Reference:

7823-50, Session 12
Mask shop automation: station controllers for photomask manufacturing
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Station Controllers have existed in Wafer fabs for well over a decade now. Until recently a need for station controllers was not keenly felt in a photo mask operation. Relatively low volume of masks produced did not justify the added cost of enabling SECS/GEM on the tools and implementing full automation.

Combination of recent factors drove the need for automation. A drive to improve first pass yield required a greater level of process control and data collection on the tools and reduction in errors in introducing lots. A push to improve the tool availability required accurate collection of data on tool events. The tipping point was reached with 32 nm processes and tools that required advanced capabilities such as excursion prevention and advanced process control.

The implementation of SECS/GEM capability on Mask equipment, have been sporadic at best resulting in range of capability depending on the equipment age and the suppliers experience with wafer fab automation. Devising a flexible system that can interface with such wide range of equipment capability has been a challenge.

Though the mask shop was able to leverage some of the middleware and framework components available to the wafer 300mm fabs, there were significant differences in the manufacturing process/flow that required architectural/code changes the various components. In addition to integrating with applications developed in-house and those available commercially. Significant effort went into the development of Dispatch application that abstracts the capabilities of the underlying MES (Workstream) with the key goals to make it possible for mask shop to migrate from legacy Workstream to newer Windows based MES in the near future.

This paper will discuss key capabilities, architectural highlights and strategies in implementation. In addition we will discuss the challenges faced and key learning in development and validation of the controllers in a full production environment with minimum impact to the processing of WIP.

7823-51, Session 12
Defect reduction through lean methodology

Lean manufacturing is a systemic method of identifying and eliminating waste. Use of lean manufacturing techniques at the IBM photomask manufacturing facility has increased efficiency and productivity of the photomask process. Tools, such as, value stream mapping, 5S and structured problem solving are widely used today. In this paper we describe a step-by-step lean technique used to systematically decrease defects resulting in reduced material costs, inspection costs and cycle time. The method used consists of an 8-step approach commonly referred to as the 8D problem solving process. This process allowed us to identify both prominent issues as well as more subtle problems requiring in depth investigation. The methodology used is flexible and can be applied to numerous situations. Advantages to lean methodology are also discussed.

7823-52, Session 12
How to match without copying: an approach for APSM mask process matching using aerial imaging
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For merchant mask makers the reproduction of a customer-provided mask process signature is a core competency as it allows customer qualification without forcing them to adjust their OPC model. This reproduction or matching of a mask process signature typically focuses on systematic CD variations driven by feature geometry, two examples are: the CD linearity (i.e. CD variation as function of feature size) or proximity behaviour (i.e. CD variations due to change of local density or distance to neighbouring structures). These signatures are driven by many aspects of mask making ranging from blank material properties, hardware set-up to unit process conditions. Therefore the task is to find a suitable combination of materials, hardware and processing that matches the desired signature.

In case of an alternating phase-shifting mask (APSM) another level of complexity is present: the phase balancing. Whereas the above mentioned CD errors are only driven by the absorber structures remaining on the mask after etching the phase balancing is determined by the quartz etch profiles. It is well known that resulting transmission and phase of an APSM mask beside etch depths also strongly depend on fine details of the quartz profiles, e.g. sidewall angles and micro-trenching [1], [2]. When setting up an OPC model all of these effects can be taken care of by relative sizing of zero and pi structures (maybe also depending on CD target), overall bias etc., the only remaining constraint is the overall etch depths as it determines the effective phase shift and so the CD behaviour as function of defocus [3], [4].

For a mask maker to match a given APSM mask without adjustment of customer OPC goes beyond mere characterization of the signature
by CD-SEM measurements. Due to above described relation between phase balancing and quartz etching this is extended into full analysis of quartz geometries, i.e. determination of etch depths, sidewall angle and micro-trenching as function of feature type and feature size. As this can only be achieved by cross-sections it is very time and resource consuming. The next step would be a fine tuning of the quartz etch process to exactly provide the same profiles. In case of experimental etch process tuning the described characterization of the quartz profiles would be required for etch set of process conditions. In sum this results in a huge amount of work and time required.

An alternative approach is to not copy the mask but to match the imaging properties of the mask [5]. In this paper we describe how this can be successfully done. In a first step a customer-provided testmask was characterized using AIMSTM measurements. This mask provides the full range of feature types and sizes as later on used for productive designs. Duplicates of this design were manufactured to set up a quartz etch process and to determine required etch depths for phase balancing using this process. On each mask only non-destructive AIMSTM and SNP-measurements were carried out to assess matching quality with the reference mask. At the end a mask process was found that yields a mask differing from the reference mask in many parameters but nevertheless mimicking their aerial images.

This duplicate was then printed in the wafer fab side-by-side with the reference mask to check the matching which was confirmed. After this confirmation a mask containing a productive design was manufactured using the same mask process. Also here a perfect match between duplicate and reference was obtained based on customer relevant wafer data.


7823-53, Session 13

Advanced laser mask repair in the current wafer foundry environment

T. E. Robinson, RAVE LLC (United States)

Contrary to the prior assumptions of its technical demise, deep UV (DUV) femtosecond pulsed laser repair of photomasks is continuing to mature and improve as a technology. Similar to the optical enhancements that allow for 193 nm wavelength light to continue being used down to the 32, or even in some cases 22, nm node, the process regimes for this type of laser repair continue to expand. This work reviews the qualification and acceptance results for another fp650 tool into production at a major wafer manufacturer. In addition to analysis for the statistical capability for the repair of hard defects, advances are shown in the area of through-pellicle repair (TRP) process development. These advances include the preferential (versus surrounding reference mask structures) removal of soft defects and the capability to remove or manipulate particles on top of a flat absorber region with no detectable removal of the absorber. These developments will further demonstrate the progressive decoupling of the laser repair spot size from the minimum technology node capability of laser repair.

7823-54, Session 13

Impact of new MoSi mask compositions on processing and repair

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The mask industry has recently witnessed an increasing number of new MoSi mask blank materials which are quickly replacing the older materials as the standard in high end mask shops. These new materials, including OMOG (opaque MoSi on glass) and A202, are driven foremost by the need to reduce feature size. The extension of 193 nm exposure to the 32 nm node has been accomplished through the use of aggressive optical proximity correction (OPC) which, due to intricate features and complex patterns, makes defect inspection and pattern transfer, cleaning and repair difficult.

In order to address the increasing difficulty in inspection that is brought about by this ever increasing feature complexity, much attention has been given to the use of OMOG which, due to it’s binary nature, demonstrates many advantages over 6% attenuated MoSi such as improved resolution and CD uniformity and an improvement in the inspectability [1,2].

Another MoSi material of interest, A202, is a high transmission (20%) material which also attempts to address the challenges presented by transitioning to smaller technology nodes. This material utilizes a thinner overall substrate stack than previous high transmission schemes allowing the resolution of smaller features and more robustness for cleaning steps. This material also eliminates process steps which leads to an increase in CD uniformity across the mask and translates to savings in time and money.

While both these materials are MoSi based materials their small compositional changes require, in some cases, a significant change in processing. Among the most impacted areas are the etch, clean and repair steps. Given the potential for defects to manifest on masks, repair is an invaluable step that can significantly impact the overall yield and lead to a reduction in cycle time [3]. The Carl Zeiss MeRiT® electron beam mask repair line provides the most advanced repair capabilities allowing a wide range of repairs to be performed on a number of mask types [4].

In a joint effort between MP Mask Technology Center LLC and Carl Zeiss SMT, this paper focuses on the benefits of the new A202 mask blank and the challenges it presents to the repair community. On site compositional surface and depth analysis was performed with a XPS on an A202 mask blank and traditional A61A in order to compare the compositional differences. Monte Carlo simulations were performed to elucidate the differences in beam interaction volume. After defining these initial differences, development of a new repair process for A202 utilizing the on-site Carl Zeiss MeRiT® MG 45 is presented along with several repairs and their AIMS results.

7823-55, Session 13

Prospect of EUV mask repair technology using e-beam tool

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Currently, repair machines used for advanced photomasks utilize principle method like as FIB, AFM, and EB. There are specific characteristic respectively, thus they have an opportunity to be used in suitable situation. But when it comes to EUV generation, pattern size is so small highly expected as under 80nm that higher image resolution and repair accuracy is needed for its machines. Because FIB machine has intrinsic damage problem induced by Ga ion and AFM machine has critical tip size issue, those machines are basically difficult to be applied for EUV generation. Consequently, we focused on EB repair tool for research work.
EB repair tool has undergone practical milestone about MoSi based masks. We have applied same process which is used for MoSi to EUV blank and confirmed its reaction. Then we found some severe problems which show uncontrollable feature due to its enormously strong reaction between etching gas and absorber material. Though we could etch opaque defect with conventional method and get the edge shaped straight by top-down SEM viewing, there were problems like as sidewall undercut or local erosion depending on defect shape. In order to cope with these problems, the tool vendor has developed a new process and reported it through an international conference [1].

We have evaluated the new process mentioned above in detail. In this paper, we will bring the results of those evaluations. Several experiments for repair accuracy, process stability, and other items have been done under estimation of practical condition assuming diversified size and shape defects. An actual printability test will be also included. This report shows not only just the results of experiment and survey but also prospect of practical use in the future. While there may be a possibility, we will extract challenging tasks and make them clear in order to ensure repair technology in the future.

Reference

7823-56, Session 13

Study of EUV mask defect repair using FIB method
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Extreme ultraviolet lithography (EUVL) is the most progressive next generation lithographic (NGL) technology after 193 nm immersion lithography. However, there are some technological issues concerning source power, particle-free mask handling, resist material development, and so on. From the view point of EUVL mask fabrication, mask pattern defect repair is one of the most difficult issues. This is since the device pattern feature size for EUVL era is smaller than that for optical lithography, a higher repairing accuracy compared with that used in optical mask is required. Looking at mask fabrication from mask pattern repair, some capabilities and problems concerning the repairing methods for EUVL mask were already reported. The FIB-GAE repair method has some advantages of repairing accuracy and field experience over other candidates.

The conventional repair process of clear defect was putting CVD film on clear defect area with the optimized width and thickness. In photomask Japan 2009, we reported the repair performance of clear defects using FIB-CVD method. In this case, the carbon based precursor was chosen as CVD material and SFET exposure results showed that the repaired pattern showed excellent exposure latitude under the condition of adequate thickness of CDV films. In addition, the results showed that the thinner CVD films deteriorate the exposure latitude.

Then we evaluated the cleaning durability of CVD films. The results showed the conventional CVD films didn’t have enough resistant to contamination-cleaning process like irradiation of VUV light, atomic hydrogen and concentrated ozone, during high volume manufacturing. In this paper, we will report the newly developed repair method of clear defects on EUV mask using FIB technique. The clear defects were repaired with removing or damaging the reflective multilayer underlying the clear defect area instead of applying the conventional FIB-CVD films. After removing the multilayer, the cross sectional pattern angle was approximately 85 degree and excellent repair performances were confirmed by SFET exposure and EUV microscope imaging.

This work was supported by NEDO.

7823-57, Session 14

Study and improvement approach to 193-nm radiation damage of attenuated phase-shift mask

The advance of exposure tool for optical lithography brings not only minute pattern formation but also throughput up. However, throughput up causes the increase of accumulation of exposure dose, which induces the mask CD growth. This issue has been reported as the radiation damage in recent years and becomes serious, because it brings the low yield of device chip due to mask CD degradation. As one solution for this issue, it was found that the radiation damage can be reduced by the ultra extreme dry air in exposure tool. Although it is effective, all exposure tools cannot necessarily adopt the ultra extreme dry air. To prolong the life of mask is one of the most important factors for the development of optical lithography and can be the big merit for device maker. That is, it contributes to the production improvement.

This work is evaluation to solve the radiation damage from not exposure atmosphere side but mask side. The attenuated phase-shift mask (att.PSM) was chosen for this evaluation because its radiation damage is severest. 193nm ArF excimer laser was exposed to att. PSM and an amount of CD degradation was confirmed by CD-SEM. Analysis was done by TEM (Transmission Electron Microscope) and EDS (Energy Dispersion X-ray Spectrometry). From the results, we inferred generative mechanism.

7823-58, Session 14

Fundamental study of droplet spray characteristics in photomask cleaning for advanced lithography
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With each technology node, smaller particles must be removed from increasing fragile photomask features such as sub-resolution assisting features (SRAF). Two dominant physical force-cleaning technologies are used in the industry today: MegaSonic and droplet-based cleaning. While both technologies continue to be studied for damage-free particle removal on silicon wafers, little fundamental work has been performed to understand the dynamics of particle removal vs. pattern damage on photomasks. Use of ion-bearing and/or aggressive chemicals for cleaning optical or EUVL masks is very limited due to concerns of surface material degradation and vacuum compatibility. Consequently, physical cleaning methods such as MegaSonic and droplet-based cleaning must be deployed to provide the highest particle removal efficiency (PRE) with zero feature damage, even in unfavorable Zeta-potential regimes.

In this study, the fundamentals of droplet-based cleaning are investigated and performance regimes that enable the use of binary spray technologies in advanced mask cleaning are identified. Using phase Doppler anemometry (PDA) techniques, the effect of key performance parameters such as liquid and gas flow rates and temperature, nozzle design and surface distance on droplet size, velocity and distributions are studied. The data are correlated to PRE and feature damage results obtained on advanced photomasks for 193-nm immersion lithography. Higher gas flow rate and lower liquid flow rate will induce more feature damage due to the stronger physical force. Higher liquid flow rate and reducing gas flow rate are the right combination to minimize SRAF damage. However, in order to meet zero SRAF damage while maintaining high PRE, it is necessary to
also optimize the photomask rotation speed and the surface distance between the nozzle and the mask.

7823-59, Session 14

Qualification of BitClean(TM) technology in photomask production

T. E. Robinson, RAVE LLC (United States)

Makers and users of advanced technology photomasks have seen increased difficulties with the removal of persistent, or stubborn, nanoparticle contamination. Shrinking pattern geometries, and new mask clean technologies to minimize haze, have both increased the number of problems and loss of mask yield due to these non-removable nanoparticles. A novel technique (BitCleanTM) has been developed using the MerlinTM platform, a scanning probe microscope system originally designed for nanomachining photomask defect repair. Progress in the technical development of this approach into a manufacture-able solution is reviewed and its effectiveness is shown in selectively removing adherent particles without touching surrounding sensitive structures. Results will also be reviewed that were generated in the qualification and acceptance of this new technology in a photomask production environment. These results will be discussed in their relation to the minimum particle size allowed on a given design, particle removal efficiency per pass of the NanoBitTM (PREPP), and the resultant average removal throughput of particles unaffected by any other available mask clean process.

7823-60, Session 14

Confirmation about degradation of capping layer in some kinds of cleaning condition

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In EUV mask lithography, it is an important issue to prevent pollution to EUV mask. Therefore, improvement of cleaning condition of polluted EUV mask is important. In EUV mask cleaning, it must be cleaned without degradation of EUV mask materials. In particular, having small degradation of capping layer and multilayer is important. There is some kinds of capping layer, those cleaning tolerance is different. Tolerance of some kinds of capping layer is evaluated by some following cleaning so far. The cleaning includes RCA cleaning, UV-Ozone cleaning and others. However, there are data which compared influence on tolerance of each capping layer. In this paper, we will compare tolerance of each capping layer. We will evaluate some kinds of cleaning method for confirmation about tolerance of some kinds of capping layers. We will confirm EUV reflectance change of multilayer due to cleaning. After that, we will analyze surface of capping layer. From these results, we will confirm influence of capping layer material for tolerance in same cleaning condition. And we will examine a cleaning condition to lower degradation of capping layer.

In addition, we will confirm cleaning ability with polluted sample. In this test, we will confirm EUV reflectance of multilayer before cleaning and after cleaning. We will estimate cleaning ability from these reflectance data.

This work is supported by NEDO.

7823-61, Session 14

Study of the airborne SO2 and NH3 contamination on Cr, MoSi, and quartz surfaces of photomasks

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Airborne molecular contaminants (AMC) in the photomask environment are a critical issue in regard with their ability to contaminate mask surfaces and then to photo-chemically evolve under DUV exposure to form crystal growth / haze [1-2,3]. These progressive defects appear as well on all materials found on the pattern-side as on the non-pattern-side leading then to drastic shortened mask lifetime, additional costs and erratic cycle time [3,4]. Among AMC, atmospheric dioxide sulphur (SO2) and ammonia (NH3) are reported as main detractors inducing significant ammonium sulphate crystal growth [5, 6]. However, the basic knowledge of the SO2 and NH3 contamination mechanisms (deposition behaviour, kinetic,...) on the different mask surfaces as the deposited amounts are not known. Such data are obviously required to control the molecular contamination at the photomask surface in order to understand and to prevent the haze generation risks.

In this paper, we have precisely investigated the deposition of the airborne SO2 and NH3 on Cr, MoSi and quartz photomask surfaces depending on the exposure time, the airborne concentration or the air humidity. Experimentally, Si-wafers covered with a mask-like Cr, MoSi or quartz layer representative of real photomasks surfaces (?) were exposed to controlled contaminated atmosphere. This experimental approach from substrates based on wafer geometry allows the quantitative analysis of SO2 and NH3 by LPE-IC (Liquid Phase Extraction and Ionic Chromatography).

By this way, first results show that Cr surfaces present a very strong ability to be contaminated both for SO2 and NH3 up to a saturation level around 1E+14 molecules/cm² in good agreement with Langmuir-type adsorption models allowing us to determine adsorption kinetic constants. On the contrary, MoSi surfaces and even more quartz layers seem slightly contaminated even at high atmospheric concentrations.

Furthermore, the air humidity effect has been addressed showing an enhancement of the contaminants deposition at clean room humidity versus drier conditions. Complement characterization (by XPS, AFM, MEB,...) have been also performed in the case of Cr contaminated surfaces allowing a better understanding of the contamination process.

To conclude, the obtained results contribute to a better understanding of molecular contamination behaviour of photomask surfaces and they will be discussed in regard to haze control perspectives.

References


7823-62, Session 15

Electron-beam inspection of NGL reticles

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This paper presents initial results from KLA-Tencor’s reticle electron-beam inspection program, applied to next-generation lithography reticles including EUV and NIL. As lithography moves to 22 nm and below, it is becoming increasing difficult to detect and disposition reticle defects using optical technology. One potential solution is to eliminate resolution issues by inspecting reticles using an electron-beam inspection system. Signal levels for defects of interest and noise levels from the reticle and the system are analyzed. Prototype system performance results for defect sensitivity and inspection throughput will be presented. Issues such as potential mask damage will be explored. Finally, the advantages and disadvantages of electron-beam and EUV inspection systems for reticle inspection will be compared.
EUV-mask defecitvity study by existing DUV tools and new e-beam technology

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While EUV lithography is approaching the pre-production stage, improving mask defectivity is recognized as the top challenge. The accepted strategy for EUV reticle qualification is the combination of a dedicated blank inspection, that should visualize the EUV-specific multi-layer (ML) type defects, and the usual patterned-mask inspection (PMI), that must be capable to meet the resolution requirements of the pattern. For the former the needs for actinic inspection is considered the strongest, in view of the limitation of optical light to visualize the nm-high distortions of the ML. Earlier publications showed that wafer inspection reveals mask defects due to the mask blank, which is too late. Yet, also existing PMI and wafer inspection tools present detection gaps in capability between printed defects and defects detected on the mask (and the blank).

In this paper we explore methods intended to close these gaps in preparation for EUV lithography high volume manufacturing (HVM). We compare existing inspection solutions for detecting EUV mask defects (193nm based mask inspection and repeater analysis in a DUV wafer inspection) and present a feasibility study for use of fast e-beam technology for mask inspection. Finally we discuss the prospects of existing DUV tools and future e-beam technology to support EUV reticle inspection on early and later nodes.

Native pattern defect inspection on 88-nm HP dense pattern using advanced electron-beam inspection system

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Fabrication of defect free EUV mask is one of the most critical roadblocks for implementing EUV lithography into semiconductor high volume manufacturing for 22nm half-pitch (HP) node and beyond. At the same time, development of quality assurance process for the defect free EUV mask is also another critical challenge we need to address. Inspection tools act important role in quality assurance process to ensure the defect free EUV mask. We are currently evaluating two types of inspection system: optical inspection (OP) system and electron beam inspection (EBI) system. While OP system is sophisticated technology and has advantage in throughput, EBI system is superior in sensitivity and extendability to even small pattern.

We evaluated sensitivity of EBI system and found it could detect 25 nm defects on 88nm L/S pattern which is as small as target defect size for 23 nm Flash HP pattern in 2013 in 2009 ITRS lithography roadmap. EBI system is effective inspection tool even at this moment to detect such small defects on 88nm HP pattern, though there are still some challenges such as the slow throughput. Therefore, EBI system can be used as bridge tool to compensate insufficient sensitivity of current inspection tools and improve EUV mask fabrication process. In this paper, we will present the results of native pattern defects found on large field 88nm HP pattern using advance EBI system. We will also classify those defects and propose some ideas to mitigate them and realize the defect free EUV mask.

Development of EB inspection system(EBeyeM) for EUV mask

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Normally, optical inspection system is used to guarantee defects of Photomask. State-of-the-arts optical inspection system has the light source of ArF area. But it is difficult for even that system to meet the defect specification of EUV mask because the pattern size of EUV mask is smaller than that of Photomask and that system cannot get sufficient pattern resolution.

SEM(Scanning electron microscope) inspection system is one of the candidate of defect inspection for EUV mask, but it takes too much time to inspect full area of EUV mask.

We are developing new electron beam inspection system, named EBeyeM, which features high speed and high resolution inspection for EUV mask. Because EBeyeM has the projection electron microscope(PEM) technique, the scan time of EBeyeM is much faster than that of conventional SEM inspection system. EBeyeM irradiates the electron beam to the area of few hundreds square um of the sample. The reflected electron signal is detected by TDI(Time Delay Integration) sensor. To get whole EUV mask image, inspection stage moves continuously.

We compared the result of EBeyeM and conventional optical inspection system. We inspected EUV blank with EBeyeM and conventional optical blank inspection system. We confirmed the number of contamination detected with EBeyeM is much more than that of conventional optical blank inspection system. And we will inspect EUV mask with EBeyeM and conventional optical inspection system.

We will report outline and performance of EBeyeM.

Study of shape evaluation for mask and silicon using large field of view

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We have developed the effective method of mask and silicon metrology using large field of view. This method is achieved by joining multi SEM images by high accuracy.

The aim of this method is evaluating the performance of the silicon corresponding to Hotspot on a mask.

As a result, the performance of the pattern in large field of view where the effect of OPC influences can be verified.

The method adopts a metrology management system based on DBM (Design Based Metrology).

This is the high accurate contouring created by an edge detection algorithm used in mask CD-SEM and silicon CD-SEM.

Currently, as semiconductor manufacture moves towsrd even smaller feature size, this necessitates more aggressive optical proximity correction (OPC) to drive the super-resolution technology (RET). In other words, there is a trade-off between highly precise RET and mask manufacture, and this has a big impact on the semiconductor market that centers on the mask business.

The verification of OPC in large field of view is important as the optimum solution for these problems.

In this study, we conducted experiments for large field of view method of the pattern (Measurement Based Contouring) as two-dimensional
mask and silicon evaluation technique. That is, observation of the identical position of a mask and silicon was considered. It is possible to analyze variability of the edge of the same position with high precision. The result proved its detection accuracy and reliability of variability on two-dimensional pattern (mask and silicon), and is adaptable to following fields of mask quality management.

- Estimate of the correlativity of shape variability and a process margin.
- Determination of two-dimensional variability of pattern.
- Verification of the performance of the pattern of various kinds of Hotspots.

In this report, we introduce the experimental results and the application. We expect that the mask measurement and the shape control on mask production will make a huge contribution to mask yield-enhancement and that the DFM solution for mask quality control process will become much more important technology than ever. It is very important to observe the shape of the same location of Design, Mask, and Silicon in such a viewpoint.

7823-67, Session 16

New strategies for mask noise reduction

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The shrinking of feature sizes printed is only partly supported by optical resolution of lithography scanners. The result effect is driving the effective resolution factor, k1, down to its physical limitations. As immersion ArF scanners are reaching their resolution limits, while alternative solutions are delayed, the pressure on reducing k1 is increasing. The result is an extreme complexity of mask design, reaching its peaks with source mask optimization, which enables driving the single patterning k1 near its 0.25 limit. With reduced k1, the amount of irregular patterns on the mask increase, and on SMO masks the amount of irregular patterns becomes the majority. The complexity of SMO patterns on a mask makes them more sensitive to process variations, and the accuracy of mask patterns is much harder to achieve. While the impact of such pattern variations may have only slight influence on the printed wafer, it becomes a challenge to inspection as it dramatically increases the mask noise.

The other side of pattern shrinking is that it increases the demand for detection sensitivity. However, mask noise competes with sensitivity demands, and mask inspectability is impaired.

Mask inspection sensitivity is limited by the ratio between the defect signal and the noise of the background (SNR). Defects with low signal (low SNR) cannot be discriminated from the background noise and thus are not detected. An effective inspection strategy should obtain good signal for the defects of interest (DOIs) and a low signal for the background noise. For that matter the noise can either come from the imaging tool (shot noise, aberrations, mechanical noise) or the mask (nuisances: writing quality, edge roughness, SRAFs). These noise sources give rise to increasing false alarm rates as attempts are made to lower the minimum detection limit during mask inspection.

Here we propose a new mask inspection concept for dealing both with the demand for increased sensitivity and the increasing amount of mask noise. We demonstrate that by combining different inspection technologies into a single inspection strategy one may obtain much more than their sum by leveraging the independent false alarm mechanisms. Enhanced detection sensitivity is achieved by suppressing mask noise to a minimum. The improved signal to noise ratio is available for all inspection flows, computational, D2D, D2DB, and is independent of the mask layout. We apply this inspection concept on advanced masks, and demonstrate its effectiveness. With this new concept, aerial mask inspection can be extended to 22nm logic node and further down to the 20nm HP frontier, soon to be faced by flash memory.

7823-68-69, Session 16

Inspection of advanced computational lithography logic reticles using a 193-nm inspection system

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Design, fabrication, and qualification of logic reticles for the 22-nm logic generation will undergo a significant leap due to new OPC technologies required to meet the wafer lithography process window demands. It is expected that computational lithographic techniques such as source mask optimization (SMO) and inverse lithography technology (ILT) will be used for several critical layers in every device. While these advanced techniques will provide larger wafer process windows, the remaining unusual reticle feature shapes and sizes will add a new level of complexity to reticle fabrication and qualification.

Traditional reticle plane inspection (RPI) is very capable for more traditional reticle feature shapes and sizes. However, RPI may be insufficient to fully inspect and qualify these challenging new reticle layouts. New techniques using lithography plane inspection (LPI) may be required.

In this paper, we report reticle inspection results of early 22-nm logic reticles incorporating computational lithography such as SMO and ILT. Inspection is performed using a state-of-the-art 193 nm reticle inspection system with both traditional RPI and the new LPI.

Evaluation includes defect detection performance using several special test reticles containing computational lithography features with programmed critical defects measured based on wafer print impact. Also included are inspection results from several full field product reticles incorporating computational lithography methods that show low nuisance defect counts. Inspection is done in both die-to-database and die-to-die inspection modes.

7823-70, Session 16

Lithographic pattern recovery (LPR) for sub-32-nm mask defect review and classification

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As optical lithography continues to extend into low-k1 regime, resolution of mask patterns under mask inspection optical conditions continues to diminish. Furthermore, as mask complexity and MEEF has also increased, it requires detecting even smaller defects in the already narrow pitch mask patterns. This leaves the inspection engineer with the option to either purchase a higher resolution mask inspection tool or increase the detector sensitivity on the existing inspection systems. In order to meet defect sensitivity requirements in critical features of sub-32nm node designs, the latter option typically results in increased nuisance (i.e., small sub-specification) defect detection by 20-40X making this option non-manufacturable.

As a solution for automatically dispositioning the increased number of nuisance and real defects detected at higher inspection sensitivity, Luminescent has successfully employed Inverse Lithography Technology (ILT) and its patented level-set methods engine to reconstruct a mask from an inspection image, and then perform simulated AIMS dispositioning on the reconstructed mask. In this technique, named Lithographic Pattern Recovery (LPR), inspection transmitted and reflected light images of the test (i.e. defect) and reference (i.e., corresponding defect-free) regions are provided to the “inversion” engine which then computes the test and reference mask patterns corresponding to these images. An essential input to this engine is a well calibrated model incorporating inspection tool
optics, mask processing and 3D effects, and also the subsequent AIMS tool optics to be able to then simulate the aerial image impact of the defects. This flow is equivalent to doing a physical AIMS tool measurement of every defect detected during mask inspection, while at the same time maintaining inspection at high resolution. What makes this product usable in mask volume production is the high degree of accuracy of mask defect reconstruction, predicting actual AIMS measurements to within ±4% CD error (worst-case) and high simulation throughput achieving processing times of ≥250 defects/min on Luminescent’s distributed computing platform. This technique enables inspection recipes to be setup based on the sensitivity required to detect small but lithographically-significant defects, not trading-off sensitivity with nuisance defect detection.

LPR is being implemented for high-volume mask inspection in production for sub-32nm immersion-based technology nodes and higher. Furthermore, this technique will be essential to the inspection of EUV masks under non-actinic conditions.

7823-71, Session 16

Computational lithography and inspection (CLI), and its applications in mask inspection, metrology, review, and repair

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At the most advanced technology nodes, such as 32nm, 22nm, and beyond, aggressive OPC and Sub-Resolution Assist Features (SRAFs) on the mask are essential for accurate on-wafer imaging; mask patterns generated by Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO) may also be necessary for production. However, their use results in significantly increased mask complexity, making mask defect disposition more challenging than ever. Computational Lithography and Inspection (CLI) have broad applications in mask inspection, metrology, review, and repair, and provide additional information to assist the operator in making accurate and efficient decisions on defect disposition. Lithography Plane Review (LPR) represents one such application of CLI for mask inspection. The original mask patterns stored by mask inspection systems can be recovered using a patented algorithm based on the Level Set Method. More accurate lithography simulation models can be used to further evaluate the defect in simulated resist patterns. An automated defect classification based on lithographic significance and local CD changes has also been developed that enables disposition of tens of thousands of potential defects in minutes, minimizing impact on inspection throughput. Another application that uses the recovered mask pattern is mask CD metrology; where the recovered mask pattern used in combination with the mask inspection image can serve as a basis for a virtual CD SEM which generates a global mask CD map of thousands of locations on the real mask pattern without needing access to CD metrology tools. In the mask repair area, one application of CLI is Reference Pattern Generator (RPG), where the simulated SEM image obtained from mask design using mask process and SEM image models can be used as the reference pattern for E-beam repair tool. In AIMSTM review, CLI can be used to close the gap between aerial image intensity and wafer resist CD, automatically dispositioning defects, and can also be extended to predict wafer CD under a different illumination source (that AIMS does not provide), such as free-form source using a patented approach. In this paper these applications of CLI in mask inspection, off-line review, metrology, and repair are presented and discussed.

7823-72, Session 17

Detecting measurement outliers: remeasure efficiently

A. Ullrich, Advanced Mask Technology Ctr. GmbH Co. KG

Shrinking structures, advanced OPC and complex measurement strategies continually challenge CD (critical dimension) metrology tools and recipe creation processes. The control of measurement outlier behavior is one important quality ensuring task. Outlier could trigger false positive alarm for specification violations impacting cycle time or potentially yield. Constant high level of outliers not only deteriorates cycle time but also puts unnecessary stress on tool operator leading eventually to human errors.

At tool level the source of outliers are the natural variations (e.g. beam current etc), drifts, contrast conditions, focus determination or pattern recognition issues etc. Some of these can result from suboptimal or even wrong recipe settings, like focus position or measurement box size. Such outliers, created by an automatic recipe creation process faced with more complicated structures, would manifest itself more systematic variation of measurements then the one caused by “pure” tool variation.

We analyzed several statistical methods to detect outlier. These ranges from classical outlier tests for extrema, robust metrics like interquartile range (IQR) to methods evaluating the distribution of different populations of measurement sites, like Cochran test. The latter suit especially the detection of systematic effects. The next level of outlier detection entwines additional information about the mask and the manufacturing process with the measurements results. The methods were reviewed for measured variations assumed to be normal distributed with a mean of zero but also for the presence of a statistically significant spatial process signature.

We arrive at the conclusion that intelligent outlier detection can greatly influence the efficiency and cycle time of CD metrology. In combination with process information like target, typical platform variation and signature one can tailor the detection to the needs of the photomask at hand. By monitoring the outlier behavior carefully weaknesses of the automatic recipe creation process can be spotted.

7823-73, Session 17

Advanced mask CD MTT correction technique through improvement of CD measurement repeatability of CD SEM

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In this study, the method to achieve the precise CD MTT (critical dimension mean to target) correction in manufacturing attenuated PSM (phase-shift mask) is investigated. There has been a growing demand for more precise Mask CD MTT control in recent years. The CD correction method has been developed and applied to meet the tighter CD MTT specification. However, the efficiency of the CD correction is greatly affected by the repeatability of the CD measurement. The factors that can have an influence on the CD measurement result are fluctuations of the pattern profile and the electron current of the SEM.

The conventional CD MTT correction method is basically to correct MoSi CD MTT by applying the additional corrective MoSi dry etch based on Cr CD value. Therefore, the repeatability of the Cr CD is the crucial point for the accuracy of the final CD MTT correction.

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7823-74, Session 17

**Improving registration measurement capability by defining a 2D grid standard using multiple registration measurement tools**

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Currently all LMS IPRO pattern placement metrology tools are calibrated using a 1D length standard provided by a national standards institute (e.g. NIST or PTB), however there are no 2-D standards available with an uncertainty matching the requirements of state of the art mask manufacturing. Therefore, the 2D stage coordinate system of the IPRO systems is calibrated using KLA Tencor proprietary combined correction technique.

With introduction of the LMS IPRO4 into high volume mask production at the AMTC, AMTC and KLA-Tencor MIE have demonstrated the capability to match IPRO3 and IPRO4 grids within 1.2 nm uncertainty. Using the golden tool approach, we could achieve a significant improvement of the pattern placement measurement capability of previous generation measurement tools of up to 30%, leading to an improved capability and thus extended useful lifetime.

The use of multiple high end registration measurement tools enables the creation of a 2D coordinate system standard, which could be used for further improved fleet matching and which would help to improve the capability of older generation pattern placement metrology tools by matching to this standard, providing the value of an extended capability and life time of the older generation tool. Within this paper different world wide fleet matching approaches (e.g. golden tool, round robin) are discussed.

7823-75, Session 17

**CD-signature determination by Nuflare inspection tool**

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Critical Dimension uniformity (CDU) is one of the most critical parameters for the characterization of photomasks. Lately it has been shown, that advanced CD (critical dimension) SEM tools and mask processes can distinguish the random short-range CD variation from the global CD signature, which is driven by stable process and design characteristics. Modern electron beam writers can utilize this global CD signature information and correct the CDU of photomasks accordingly. Therefore a detailed knowledge of the signature will benefit strongly photomask CDU.

The current process is to rely primarily on CD signatures derived from CD SEMs. This has the major shortcoming that with higher resolution of the signature the cycle time at metrology is prolonged. The trade off is a CD resolution somewhat around one cm. Even then the photomask will have to stay a substantially percentage of the total cycle time at a non-value added process step.

In this paper we will argue that the solution to this dilemma can be found at a completely different process area - at inspection. We will present data that show that the novel CD map feature of the NPI inspection tools enables CD maps in unparalleled resolution in the mm region. They far exceed what CD SEMs are capable of even at 100fold of current measurement times and utilize a tuneable spectrum of different features and hence are not limited to “good” CD measurement sites. To make matters even better, the CD map is generated in parallel to the traditional inspection. It has no impact on cycle time and works for pre- and post pellicle inspections equally well.

To challenge the method we used a single die layout of a current logic design and referenced all data only to database. Nevertheless, the data presented will demonstrate the excellent repeatability of the CD map measurement and the very good matching to CD SEM measurements (the limitations to perfect were primarily due to CD SEM measurement site availability).

7823-76, Session 17

**In-die registration metrology: design data preparation solution**

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Double Patterning Lithography (DPL) for next generation wafer exposure is placing greater demands on the requirements for pattern placement accuracy on photomasks. Recent studies have shown that pattern placement accuracy can be the largest component of systematic wafer overlay error after the scanner. Since LELE or LFLE DPL technologies tighten intra-field-wafer overlay requirements by as much as a factor of two, to 2 - 3nm for critical layers, minimizing all sources of systematic overlay error has become critical. In addition to its impact on overlay performance, any significant pattern placement between the two exposures in a double patterning scheme will have a significant impact on CD uniformity, another major area of concern for next-generation devices.

In the past, mask registration has been referenced to design data using relatively large, specially designed targets. However, as shown in many previous papers, the true registration error of a next-generation reticle cannot be sufficiently described by using today’s sampling plans. In order to address this issue, it is mandatory to have in-die registration capability for next generation reticle registration. On this path to in-die pattern placement metrology many challenges have to be solved. One is the data preparation necessary to get the targets placed and marked within the design, preparing for the later metrology step.

In this paper we will demonstrate an automated way of performing in-die registration metrology. This new approach allows more flexible and higher density metrology so that pattern placement error is sufficiently well characterized.

7823-77, Session 17

**Improving registration metrology by correlation methods based on alias-free aerial image simulation**

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The increased industry requirements for pattern registration tools in terms of resolution and in-die measurement capability lead to the development of the new photomask registration and overlay metrology system PROVETM at Carl Zeiss. Performance measures of the tool are actually driven by double exposure/ double patterning approaches which will help to extend the 193nm lithography platforms while keeping the semiconductor industry conform to ITRS roadmap requirements. To achieve the challenging specifications, PROVETM features beside a highly stable hardware system new image analysis methods which are designed to meet the requirements both for standard markers as for in-die features.

For that, in addition to conventional threshold-based image analysis, PROVETM will provide a more accurate correlation analysis to measure pattern placement errors with respect to design images. This correlation is based on an aerial image simulation of the
corresponding reference design patterns. Since reproducibility and accuracy specifications at camera level are far below the pixel size of the CCD, sophisticated algorithms have to be used to avoid super-pixeling effects. It will be shown that super-pixeling effects of discretized design images will affect the placement accuracy or to unrealistic small design pixel dimensions, connected with huge image sizes. The solution is an alias-free forward transform that performs the discretization in Fourier space and will not disturb the pattern placement. It is indicated by simulations that this allows the detection of an arbitrary sub-pixel placement error with high accuracy. Furthermore, it is demonstrated that correlation methods reduce the impact of camera noise compared to threshold methods, in particular for small in-die features as contact holes.

7823-78, Session 18

Using principal component analysis for photomask CD signature investigations

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The reduction of dimensions in integrated circuit designs, coupled with increases in circuit density has led to stringent criteria in both wafer and photomask manufacturing. Of particular interest is reticle critical dimension (CD) error, which must be controlled to the contribution of this error with smaller photomask CD uniformity requirements with each new technology node. Mask makers are thus forced to reduce both the statistical and systematic CD uniformity errors, such as center to edge and side to side effects.

Often the sources of CD uniformity errors are known to mask makers and can be corrected, for example, by optimization of resist bake and/ or develop processes. For unknown sources of CD uniformity errors feedback control of reticle error can be employed. All of these methods have some success in improving CD uniformity however, sub 45nm wafer technology nodes require mask manufacturers to reliably deliver <2nm 3 . Meeting such tight CD uniformity specifications will require novel approaches for mask makers to elucidate the source of CD errors as well as eliminate or minimize their impacts.

To this end, the AMTC began an examination of CD uniformity signatures using principal components analysis (PCA), a useful statistical technique for revealing patterns in large data sets. While PCA examines only variations in a data set the resulting components of this variation point to reticle CD error sources and subsequently, to potential correction strategies. PCA was conducted on resist CD measurements in two populations of test reticles exposed with 50kV e-beam pattern generators using positive and negative chemically amplified resists (CAR). PCA was effective in identifying systematic photomask CD errors which were not evident by other examination methods. Furthermore, PCA was utilized to determine the effectiveness of CD signature matching with alternate processes and/or tools such as develop and post exposure bake (PEB).

This report presents AMTC’s application of PCA to investigate photomask CD signatures with the corresponding results.

7823-79, Session 18

Performance evaluation results on 2x nm node enabler for mask registration metrology

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Wafer overlay requirement for the 32nm DRAM HP node volume production is targeted at 6.4 nm in 2013. Consequently, this is placing significantly tighter demand on the pattern placement accuracy on photo masks at or below 4nm (3sigma /ITRS Roadmap 2009 update).

In Double Patterning Lithography (DPL) Technique case, the pattern placement specification of dependent layers is even <3nm, due to ITRS roadmap.

Besides mask litho tool registration stability, the distortion influence of the pellicle on plate bending is also a contributor especially when the pellicle distortions are not repeatable substrate to substrate. The combination of increased demand for greater accuracy and the influence of pellicle distortions are key factors in the need for high resolution through pellicle in-die measurements on actual device features.

A new registration metrology tool dedicated for the 32nm HP node and beyond is under final development. Actual measurement performance data of the beta evaluation system will be provided to verify registration metrology capability on 32nm HP node reticle manufacturing and thus to ensure to keep the reticle contribution to total wafer overlay within the required tolerances.

7823-81, Session 19

Advanced cleaning of nano-imprint lithography template in patterned media applications

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As the magnetic storage industry roadmap calls for aggressive terabit/ in2 densities over the next few years, the shift from the current planar media to patterned media; grooved surfaces (discrete track media / DTM) and/or individually defined magnetic dots (bit patterned media / BPM), will be necessary. Both types of patterned media require lithography to produce the pattern on the disk and the most promising lithography candidate today is nano-imprint lithography (NIL). During the imprinting process a thin, round, transparent template made of quartz is functioned as a mold to inversely transfer the features from its surface to the patterning medium on the disks by direct contact. One issue with this technique is the high probability of defects due to repeated contact of the template with the resist before, during, and after UV radiation. Defect management through template cleaning, inspection and defect characterization is critical to preserve integrity of the process.

In this paper, advanced acid-free cleaning combined with megasonic treatment for defect elimination is investigated for effectiveness on discrete track recording (DTR) patterned templates. For the experiments, templates containing 250KTPI (100nm track pitch) full surface DTR pattern and 450 KTPi (56nm track pitch) with narrow band DTR pattern are used. The effect of megasonic cleaning on the pattern integrity of fragile features is studied. General characterization of defect attributes is made feasible through a series of imprinting and template cleaning cycles focused on resist residues and contaminant removal. Imprinted disks are analyzed using Candela disk inspection and SEM imaging of the pattern. Template cleaning is performed using Hamatech MaskTrack automated template cleaning system.

7823-144, Session 19

Technology roadmap for hard disk drives: strategic positioning of patterned media

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The areal density limit for granular recording media has been described as a trilemma between the conflicting requirements of media SNR (favoring smaller grains), thermal stability (favoring larger grains and/ or higher anisotropy), and writeability (favoring lower anisotropy).
However, while recent innovations like exchange coupled composite (ECC) media and shingled recording have improved writeability, the anticipated SNR gain from smaller grain size is proving difficult to realize, potentially limiting density even before the trilemma is reached. Bit patterned media (BPM) is uniquely positioned to replace granular media, because density does not depend on grain size. BPM recording density is limited primarily by the island switching field distribution (SFD) and the available write field gradient. Recent advances in magnetic films and BPM ECC structures have improved the prospects for BPM in the 1-2 Tbit/in² regime and new ideas like exchange bridge films (or “capped” BPM) may further extend density. Thermally assisted recording (TAR) stands as an alternative to BPM, but requires successful development of small grain high anisotropy granular media with the proper thermal properties. Recent progress in FePt films indicates a fruitful direction for further research, which, if successful, could delay the need for BPM. On the other hand, the difficulty of developing granular TAR media can be circumvented by combining BPM with a TAR head, which may offer the ultimate in magnetic recording density. This BP-TAR combination has already demonstrated 1 Tbit/in², and may be the best solution beyond 2-5 Tbit/in².

7823-145, Session 19

Magnetic recording beyond 1 Tdpsi: a patterned media perspective


Areal density growth continues to be the key focus of magnetic recording industry to achieve ever higher-capacity and lower-cost hard disk drive. As extending perpendicular media recording becomes increasingly challenging, many new technologies are proposed and investigated, namely single-write recording, discrete-track media recording, heat-assisted recording and bit-patterned media. Single-write and discrete-track media recording are considered one-time extension for perpendicular media technology. Heat-assisted recording and/or bit-patterned media offer more extendibility but are much more difficult to underpin for productization. Both will require substantial development efforts to reach maturity. For patterned media to be viable, it is critical to meet stringent lithography requirements at > 1Tdpi and at the same time achieve low-cost objective. In addition, many drive system integration issues, e.g. track following, write timing synchronization, skew, tribology, etc, need to be resolved. From lithography perspective, di-block-copolymer technology is the only viable path to achieve the required size and pitch sigma beyond 1Tdpi. It is shown to be potentially extendible to 10Tdpi. However, this technology has limited skew capability and causes some challenges in servo pattern integration. These will need to be addressed by some innovative drive system solutions. To achieve low-cost objective, template replication and nano-imprint lithography are critical elements, which can not be over-emphasized. Metrology poses another challenge to achieve proper critical dimension control at beyond 1Tdpi density. While most of these issues are considered engineering challenges, it does demand extensive engineering resources and capital investment to achieve technology maturity for production.

7823-146, Session 19

Patterned media etch processing: a manufacturing approach

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As the HDD industry begins to see the limits of planar granular PMR recording a new recording technology will be required to continue the increasing demand for storage capacity. One such approach is based on physically patterning the recording media. The success of solution will depend on availability of capital equipment capable of processing the immense number of disks required to meet the drive requirements in an efficient, high productivity and cost effective manner. This paper will review the current status of the development of high throughput media etching and planarization equipment based on the Intevac 200 Lean disk media deposition system. The following etch-based processes have been integrated on the system currently in use at HGST: Desum resist, Hardmask opening, Magnetic layer etching and Hardmask removal. Two etching sources are in use, a CCP (Capacitive Coupled Plasma) source and an ICP (Inductively Coupled Plasma) source. A combination of Ar, Fluorinated gases, H2 and CO2 plasma etch processes are being used and etch rates of about 2.5 nm/sec have been achieved. Unit process flow data as well as magnetic recording performance of disks made on this system will be presented.

7823-148, Session 19

Challenges and promises in fabrication of bit patterned media

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One of the potential technologies for future hard disk drives is the use of bit patterned media. As is the case with all future technology candidates, including heat assisted magnetic recording (HAMR) and microwave assisted magnetic recording (MAMR), there are many challenges in fabricating bit patterned media. In particular, future ultra-high area density applications require patterned magnetic bits to be at sub-10nm dimensions. Etching at these scales is difficult to achieve with conventional ion milling techniques. Instead, reactive ion etching (RIE) techniques must be developed to meet the challenge. In this talk, we will present research on the development of a methanol based RIE scheme for fabricating bit patterned media at ultra-high area densities. We will discuss the ability of methanol RIE to etch magnetic and nonmagnetic films in the parallel plate and inductively coupled plasma (ICP) RIE configurations. We will also discuss the advantages of both configurations over straight Ar ion milling, including enhanced selectivity, minimal redeposition, and less etch induced damage or erosion. Using methanol RIE, we have demonstrated the ability to etch sub-20nm features in commercially available CoCrPt based perpendicular recording media and NiFe, as well as films related to applications in HAMR and MAMR with selectivity greater than 10:1 relative to mask materials, such as Ta, TaNx, Ti, and SiNx. These results, the promises of such a technique and the feasibility of sub-10nm dimensions will be discussed in detail throughout the talk.
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General Information

Registration

Onsite Registration Hours
Monterey Conference Center - Portola Lobby
Monday 13 September .......................... 7:30 am to 4:00 pm
Tuesday 14 September ........................ 7:15 am to 4:00 pm
Wednesday 15 September ..................... 7:30 am to 4:00 pm
Thursday 16 September ....................... 8:00 am to 10:30 am

Exhibition Hours
Monterey Conference Center – Serra Grand Ballroom
Tuesday 14 September ......................... 10:00 am to 4:00 pm; 6:15 pm to 7:45 pm
Wednesday 15 September ..................... 10:00 am to 4:00 pm
Exhibition admission is included in your registration fees.

Attendee Services

Cashier
SPIE cashier can assist with registration payments, adding a course, receipts, and badge corrections.

Internet Services

Internet Pavilion
Monterey Conference Center, Steinbeck Lobby
Sponsored by

Tuesday and Wednesday ....................... 7:30 am to 6:00 pm
Thursday ........................................... 8:00 to 10:30 am
SPIE will have a complimentary Internet Pavilion Tuesday through Thursday, 14-16 September, where attendees can use provided workstations or hook up their laptop to an Ethernet connection to access the Internet.

Wireless Internet Service
Monterey Conference Center, Exhibition Hall
Sponsored by

Open during Exhibition Hours
Complimentary wireless access is available in the Exhibition Hall, Serra Ballroom. Wi-Fi access instructions are available in the Exhibition Hall and at the SPIE Registration Desk. SPIE recommends that you properly secure your computer before accessing the public wireless network. Failure to do so may allow unauthorized access to your laptop as well as potentially introduce viruses to your computer and/or presentation.

Hotel Service Internet
Each hotel room is equipped with data ports for hook-up to high speed Internet service for $12.95 for 24 hours.

Business Services

Business Center
At the Monterey Marriott, attendees may use their hotel room key to access the onsite Business Center which offers use of a free online computer. Copy and fax machines are available at the front desk. Copies are free for the first 20 copies, 10 cents per page after. The fax machine is $1.00 per page for domestic usage and $3.00 per page for international usage.

Offsite Business Center
Fedex Kinkos is located at 799 Lighthouse Ave., Ste. A, Monterey, California, 93940, Phone: 800 463 3339. It is 1.3 miles from the Monterey Marriott (approx. 5 minutes driving time). Go north on Calle Principal, left onto Del Monte Ave., right onto Pacific St., right onto ramp to merge onto Lighthouse Ave.

Message Center
SPIE has an urgent message line available during registration hours, Monday through Thursday (831 646 5312).

Speaker Presentation Preview Room
Monterey Conference Center, Sloat Room
Open during Registration Hours
Each conference room will have a computer workstation, LCD projector, screen, lapel microphone, and laser pointer. All presenters are encouraged to visit the Speaker Presentation Preview Room to confirm display compatibility of their presentation, whether using a memory device or laptop, with the audiovisual equipment supplied in the conference rooms.

Speakers, who have requested equipment prior to the request deadline, are asked to report to the SPIE Registration Desk to confirm their requested equipment.

Course Materials Desk
Located at the SPIE Registration Desk, Open during Registration hours. If you have registered to attend a course, you will obtain your badge, course notes, and the class location during the Registration process.

Marketplace and Souvenirs
The SPIE Marketplace is your source for the latest SPIE Press books, Proceedings, and Educational and Professional Development materials. To purchase any Marketplace materials or become an SPIE Member, please ask at the Photomask Registration Desk.

Child Care Services
The Monterey Marriott suggests the following child care service companies in Monterey:
Parents Time Out, Phone: 831 375 9269
Corporate Kids Events, Inc & VIP Babysitting Services,
Phone: 800 838 2787, www.corporatekidsevents.com,
Email garen@corporatekidsevents.com
SPIE does not imply an endorsement or recommendation of this service. It is provided on an “information only” basis for your further analysis and decision. Other services may be available.
Special Events

**Exhibition Poster Reception**
*Monterey Conference Center, Serra Grand Ballroom*
Tuesday 14 September . . . . . . . . . . . . . . . . . . . . . . . . 6:15 to 7:45 pm

Hors D’oeuvres Sponsored by

[Logo: Applied Materials]

Beer Sponsored by

[Logo: Synopsys]

Symposium attendees and guests are invited to attend an Exhibition/Poster Reception on Tuesday evening in the Serra Grand Ballroom. The reception provides an opportunity for attendees to meet colleagues, network, and view poster papers. Refreshments will be served. Attendees are requested to wear their conference registration badges.

**Poster Viewing**
Tuesday 14 September . . . . . . . . . . . . . . . . . . . . . . . . 6:15 to 7:45 pm
Wednesday 15 September . . . . . . . . . . . . . . . . . . . . . . . 10:00 am to 3:00 pm

Poster authors may set up their poster papers between 10:00 am and 4:00 pm on Tuesday and will leave them up until Wednesday afternoon. Authors will be present during the Poster Reception 6:15 to 7:45 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any papers not removed by Wednesday at 3:00 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3:00 pm.

**Food & Beverage Services**

**Breakfast Breads**
*Monterey Conference Center, Steinbeck Lobby*
Complimentary breakfast breads will be served from 7:30 to 8:30 am, Tuesday through Thursday, for symposium attendees in the Steinbeck Lobby.

**Coffee Breaks**
Complimentary coffee will be served at the following times and locations. Please check the individual technical conference listings for exact times and locations.

*Monterey Conference Center, Serra Grand Ballroom*
Tuesday 14 September . . . . . . . . . . . . . . . . . . . . . . . . 10:10 to 10:40 am; 3:00 to 3:30 pm
Wednesday 15 September . . . . . . . . . . . . . . . . . . . . . . . 10:00 to 10:30 am; 3:00 to 3:30 pm

*Monterey Conference Center, Steinbeck Lobby*
Thursday 16 September . . . . . . . . . . . . . . . . . . . . . . . . 10:00 to 10:30 am; 3:00 to 3:30 pm

**SPIE-Hosted Lunches**
*Monterey Marriott, San Carlos Ballroom*
Hosted lunches will be served at the following times:

*Tuesday Lunch Sponsored by DNP America, LLC*
Tuesday through Thursday . . . . . . . . . . . . . . . . . . . . . Noon to 1:00 pm

Please check the individual technical conference listings for exact times. Complimentary tickets for these lunches are included for full conference registrants. Exhibitors and students may purchase tickets at the SPIE Registration Desk in the Portola Lobby.

**Deserts**
Dessert will be served during afternoon coffee breaks on Tuesday and Wednesday in the Exhibition Hall. A complimentary ticket for dessert will be included in attendee and exhibitor registration packets.

Special Session on EBDW/ML2

**13.5 nm or 17.3 Picometer? Are We Funding the Right Wavelength/Technology?**
*Room: Steinbeck Forum*
Wednesday 15 September . . . . . . . . . . . . . . . . . . . . . . 8:00 am to 5:30 pm

See page 5.

**Photomask Reception**
*Monterey Marriott, San Carlos Ballroom*
Wednesday 15 September . . . . . . . . . . . . . . . . . . . . . . 6:00 to 8:00 pm

Beer/Wine Sponsored by

[Logo: Hoya]

Don’t miss it! Make plans to join your colleagues and friends at the annual Photomask Reception. This year’s event focuses on good food, beverages, and plenty of time to socialize or talk business with fellow conference attendees. Awards and other presentations will be included in the evening. Admission is included with your paid registration. Guest tickets may be purchased with your pre-registration or onsite (we highly recommend purchasing in advance to assure your reservation).
Policies

Refund Policy
There is a $40 service charge for processing refunds. Requests for registration refunds must be received no later 2 September 2010. All registration fees will be forfeited after this date.

Membership dues are not refundable. SPIE Digital Library subscriptions are not refundable.

Audio, Video, Digital Recording Policy

Meeting Rooms and Poster Sessions
For copyright reasons, recordings of any kind are strictly prohibited without prior written consent of the presenter in any conference session, course or of posters presented. Each presenter being taped must file a signed written consent form. Individuals not complying with this policy will be asked to leave a given session and asked to surrender their film or recording media. Consent forms are available at the SPIE Registration Desk.

Exhibition Hall
For security and courtesy reasons, photographing or videotaping individual booths and displays in the Exhibit Hall is allowed ONLY with explicit permission from onsite company representatives. Individuals not complying with this policy will be asked to surrender their film and to leave the exhibit hall.

Laser Pointer Safety Information
SPIE supplies tested and safety approved laser pointers for all conference meeting rooms, and for course rooms if instructors request one. For safety reasons, SPIE requests that presenters use our provided laser pointers available in each meeting room.

Underage Persons on Exhibition Floor
For safety and insurance reasons, no persons under the age of 16 will be allowed in the exhibition area during move-in and move-out. During open exhibition hours, only children over the age of 12 accompanied by an adult will be allowed in the exhibition area.

Unauthorized Solicitation
Any manufacturer or supplier who is not an exhibitor and is observed to be soliciting business in the aisles, or in another company’s booth, will be asked to leave immediately. Unauthorized solicitation in the Exhibit Hall is prohibited.

Unsecured Items
Personal belongings such as briefcases, backpacks, coats, book bags, etc., should not be left unattended in meeting rooms or public areas. These items will be subject to removal by security upon discovery.

About Monterey
Monterey Marriott Hotel
350 Calle Principal
Monterey, CA 93940

The Monterey Marriott Hotel is located with in easy walking distance of the Monterey Bay Aquarium, Fisherman’s Wharf, Cannery Row and fabulous shopping. The hotel features an outdoor pool, day spa, fitness center, and nearby golf, tennis and beaches. Your hotel concierge will be happy to arrange everything from car rentals to a golf outing.

Parking

Parking at the Monterey Marriott Hotel
Valet only is available at $20 overnight (subject to change). No self parking available. Short term parking, 4 hrs or less, is $12.

Parking at the Monterey Conference Center
Public parking is available in the East Garage, two blocks down from the hotel. Drive down Franklin Street (one-way), turn left on Washington Street, and turn left into the parking garage. You can also enter the parking garage turning left on Del Monte Street or left on Tyler Street (both one way streets). To park, pay the flat rate per day of $7, payable in exact change as there is no attendant on duty to make change. MasterCard or Visa is also accepted. No in/out privileges. City Parking Lots (831-646-3953) http://www.monterey.org/parking/

Parking is also available in the West Garage across from the East Garage, which has an attendant on duty, open 24 hours with in/out privileges. Drive down Washington Street; go left on Del Monte Street and left on Tyler. The lower level has a time limit maximum of 90 minutes and parking in this lower level is free. The upper level charges $.50 per 20 minutes and $10 max per day, with the first hour free. They accept cash or American Express, MasterCard or Visa, and the attendant will make change.

Additional Conference Center Parking at the Portola Plaza Hotel Lot
Conference Center guests can park at the Portola Plaza Hotel for $2 for the 1st hour, $1 each additional half hour, maximum $20 per day payable with cash or credit cards (no checks). There is an attendant onsite. Portola Plaza Hotel phone number is 831 649 4511. The hotel is directly across from the Marriott, and both are connected to the Monterey Conference Center by a footbridge.

All parking rates are subject to change without notice.

Car Rental
Hertz Car Rental has been selected as the official car rental agency for this Symposium. To reserve a car, identify yourself as a Photomask Conference attendee using the Hertz Meeting Code CV# 029B0014.

• In the United States call +1 800 654 2240
• Book online www.hertz.com
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