The semiconductor industry is in a period of unprecedented change. The pressure to follow Moore's Law has created physical and economic challenges that often seem insurmountable. Silicon feature sizes—and even the spaces between them—are smaller than the wavelength of light used to pattern them on silicon. Once chips are patterned, the materials issues and electrical characteristics of particular lithographically produced structures can dramatically alter chip performance and reliability.

These lithography and materials effects combined to become a critical hurdle at the 130-nm process node that recently went into volume production. Yields went into a tailspin, data volumes rose exponentially, mask costs increased, and production ramped up much more slowly than anticipated. The challenges experienced at this node have implications for the future. At the 90-nm and 65-nm nodes, new lithography equipment, mechanical stress, materials effects, and overall process complexity will make high yields even more difficult to attain. Fortunately, the industry is already preparing the path to these challenging nodes. With change comes opportunity, and the innovation is already occurring to take advantage of these opportunities.

Design teams typically focus on production of a chip design ("tape out") database that has been simulated and verified to have specific timing performance and reliability. New generations of microchips require a more detailed design approach if the semiconductor industry is to keep Moore's Law alive.
power consumption. Achieving tapeout has traditionally been viewed as the end of the design team’s responsibility; yield issues have been the domain of manufacturing teams. In the past, the impact of specific design characteristics on yield and performance have been covered by design rules that give design teams minimum and maximum relative spacing between different design features. It is difficult to solve many significant yield issues only through design rules, however. At the 130-nm node and below, this approach is not sufficient. The characteristics of a given design, including feature type, spacing, and placement, can now dramatically impact both chip manufacturability and yield.

If manufacturers try to manage lithography resolution by altering a database after the design team has approved it, the chip may not perform as expected. The answer lies in breaching the wall that separates the design team from the manufacturing team and combining their expertise through a process called design intent.

**Cost Control Through Design Intent**

A significant issue for many companies moving to 130 nm and beyond has been the cost of advanced photolithography masks, which are essentially templates that bear the chip designs that will eventually fill a wafer. The average 130-nm-node commercial mask set costs $750,000, and mask-set costs for the 90-nm node are predicted to exceed $1 million.

The primary cost of a mask set is determined by mask-write time. A mask-write tool costs $15 to $20 million and must be amortized over its write times. For very advanced masks such as those used to create the smallest features on a 130-nm lithography exposure tool, the mask writer “shoots” each rectangle of the mask individually. The time to write these masks is directly proportionate to the number of rectangles into which a design must be segmented.

At the 130-nm node, approximately 70% of the masks for a single IC use optical proximity correction (OPC). In this approach, small OPC features are applied to the mask in order to compensate for the optical distortion created by the physical limitations of the lithography exposure tool, making the imaged silicon wafer more closely match the intent of the original design layout (see sidebar). To determine where OPC must be used, design rules include a certain tolerance that defines the maximum difference between an image and a layout.

Today, the standard practice is to apply OPC with the same tolerance across an entire chip layer. Tapeout teams generally set this tolerance to the minimum in order to improve the fidelity of a silicon image. This broad-based application may increase file size exponentially, and therefore, the cost of the photomask (see figure 1). Not every shape on a given layer requires such a correction, however; for example, wide wires will print better than a critical transistor with smaller features. Typically, OPC software tools have not had the ability to distinguish between the two.

Fortunately, designers have the ability to define localized tolerances in OPC application. By knowing which features are going to be most critical to chip functionality (design intent) and which features are most likely to encounter lithography issues as a result of the physical characteristics of the substrate material, designers can define a tighter or looser margin for OPC application. Using this margin, a user can perform design-driven OPC that minimizes the number of OPC features required to meet lithography goals, keeping photomask costs to a minimum.

Using design intent, a group applying OPC to a photomask...
The Corrections

Optical proximity correction (OPC) applies systematic changes to photomask geometries to compensate for nonlinear distortions caused by optical diffraction and resist process effects. These distortions include linewidth variations dependent on pattern density, which affect device-operating speed, and line-end shortening, which can break connections to contacts.

In OPC, small changes to the IC features make up for the distortions. To compensate for line-end shortening, the line is extended using a hammerhead shape that produces a line much closer to the intended shape. To compensate for corner rounding, serif shapes are added to (or subtracted from) corners to produce more accurate angles. Determining the optimal type, size, and symmetry (or lack thereof) is complex and depends on neighboring geometries and process parameters. Properly implementing OPC typically requires sophisticated software routines. —S.R.

Improving Inspection

In addition to reducing the costs of cutting-edge photomasks, a design-margin approach using an intelligent OPC application can improve mask-inspection criteria. Like the technologies used to create the photomasks and microchips, quality assurance tools such as mask and wafer inspection systems are both costly and challenging. Today, mask and wafer manufacturers must inspect millions of features on a single mask or on a single wafer. As in the case of mask writing, the tools used to perform inspections are very expensive and must be used effectively.

Today, inspections are done in as “black box tests,” which is a phrase made popular by software engineers who test software without knowing anything about its internal workings. In lithography, the term refers to the cases in which a wafer or mask inspection tool uses the same level of scrutiny across a given photomask.

As one might expect, the mask and wafer inspection process improves greatly with the use of a combination of margin, which determines the lithography impact of a given feature, and design intent. This dual approach allows an inspection operator to discriminate between a company logo on a chip and a critical transistor (see figure 2). Knowing, for example, that feature ‘A’ is in a more critical area than feature ‘C’ tells the operator to do a highly sensitive and time-consuming inspection only in the area around feature ‘A,’ performing a more relaxed inspection on other areas of the chip that are less likely to impact the end lithography result.

To perform this type of intelligent inspection, manufacturers need to understand the relative importance of features as determined by the design team. The design team may need to retain confidentiality about aspects of the design, however. To help preserve the integrity of the intellectual property inherent to the chip design, design-intent information should thus be passed forward through the tools and models that are used to perform tapeout and carry the design through manufacturing.

By adopting a more design-driven approach to production, many of the yield and manufacturing issues daunting the semiconductor industry can be addressed before they even occur. Looking forward to the 90-nm and 65-nm process nodes, these design-driven approaches will only become more critical. Smaller linewidths and tighter pitches between lines lead to a host of mechanical stress, signal integrity, photomask and lithography challenges that will have to be addressed with intelligent design. By integrating these approaches in their process today, design and manufacturing teams can not only prepare current projects for success, but also set themselves up for the future.

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