Consortium tests the viability of nanoimprint lithography

Matt Malloy

Sematech’s program evaluates the technology for making next-generation semiconductor devices and aims to drive key improvements.

Nanoimprint lithography (NIL) holds promise for patterning the small features of tomorrow’s microchips. But, will it become a major semiconductor manufacturing technology or just be a novelty? Some argue it is an obvious choice for chip makers to continue down the path of Moore’s Law, the doubling of the transistor density every two years. NIL is already used with high-density disk drives. But others view it as a curiosity, and not a legitimate threat, to mainstream approaches such as extreme UV or double patterning. Both sides have valid points, which is why Sematech, a consortium of chip manufacturers, set up its Nanoimprint Program to evaluate NIL. Our goal is to determine whether it is viable for manufacturing next-generation, 22nm-node semiconductor devices. To make our evaluations, we purchased an Imprio300 imprint system from Molecular Imprints Inc. in late 2008.

NIL users typically show excellent results patterning small features with low line-width roughness (LWR). We are able to routinely print 28nm features with approximately 2.5nm LWR (see Figure 1). The equipment is also relatively simple and replacement parts affordable compared to alternatives. For example, it uses a simple mercury arc lamp as a light source.

However, both wafer defects and overlay (the pattern position in relation to underlying layers) require significant development to reach the levels required for production. The initial capital for an imprint tool is low, but costs for the imprint mask or template currently are too high. The final template form factor has yet to be determined. And, difficult aspects of production, such as particles and contamination, are even greater issues with imprint due to the contact nature of the technology. We have already begun investigating some of the critical issues associated with nanoimprint, with initial work concentrating on improving the overlay to meet International Technology Roadmap for Semiconductors (ITRS) specifications.

Figure 1. Scanning electron microscopy image of 28nm line spaces made by nanoimprint lithography.

Still, imprint tool manufacturers such as Molecular Imprints, EV Group, Nanonex, and Obducat, have been making steady progress. Two companies stand out when it comes to overlay control. The Molecular Imprints Imprio300 system is specified at a 35nm overlay across 300mm wafers on a 32×26mm field, but it performed far better during our acceptance testing. In addition, EV Group claimed <35nm overlay on a test platform specified at 50nm. While these results fall short of the 7nm target of the ITRS for the 22nm technology node, they nevertheless show progress.

We are currently in a joint development project with Molecular Imprints to improve the overlay on the Imprio300. The acceptance test was completed successfully in November 2008 with a mean +3σ overlay performance of 24nm. The test

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Figure 2. The best single-wafer performance for overlay—the position of a pattern in relation to underlying layers—was just above 17nm.

demonstrated alignment and imprinting on top of wafers previously patterned using an ASML 1900i immersion lithography system. We showed the acceptance test results and our earlier work at SPIE 2009. The best single wafer overlay result obtained so far was just above 17nm (see Figure 2). However, the tool typically performs in the 20–30nm range (64 fields, 32x26mm per field). The final goal of this project is to consistently imprint wafers on film stacks with overlay results of <17nm.

We chose films to represent imprinting of the active, gate, and contact layers by aligning to zero-layer marks created with a shallow trench isolation process. Stretch goals include imprinting a contact layer aligned to the gate layer and a metal 1 layer (the first patterned metal layer) aligned to the contact layer. The project addresses both mix-and-match and tool-to-self overlay strategies.

While overlay is currently the main focus of our imprint program, several other projects are in the works. These include defect studies such as electrical testing, template cleaning and lifetime studies, and collaboration on development-grade templates. We are also pursuing the difficult task of imprinting without an added street between each field and thinning the residual layer thickness. Routine data collection off the Imprio300 is another important aspect of this program. The tool is in a development setting, but it is maintained and monitored as if it were in a production fab. We continually track and report overlay and critical dimension statistical-process control, particle adders, uptime, downtime, and utilization. The data will eventually be used to assess imprint tool performance and stability.

In addition, our consortium member companies and the Lithography Division’s associate members can access to the system for their own experiments and learn from our work.

The semiconductor industry needs an unbiased assessment of nanoimprint lithography. We believe Sematech can provide that. The overlay joint development work will continue into the first half of 2010, at which time another key concern for this technology will be chosen and moved to the forefront. Imprint lithography has shown its potential, but still has a long way to go to show it is a viable candidate for production at the 22nm technology node. Even if the overlay and defect hurdles are cleared, the greatest roadblock may be the industry’s willingness to accept NIL as a viable solution.

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