Double-patterning-compliant split and design

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The advanced solutions needed to produce future generations of microchips with acceptable yield require rethinking their design-layout criteria.

The challenge currently facing the semiconductor industry is to manufacture ever smaller and cheaper transistors while increasing microchip functionality. Up to now, photolithography has been a key enabler of the technology scaling required to meet future needs. However, smaller chips require a pattern period, or pitch, that makes dense features difficult to resolve using conventional approaches. Consequently, efforts have focused on ways of enhancing existing manufacturing methods. For example, water-immersion lithography improves imaging resolution to near the current optical limit of 72nm pitch. However, newer, better technologies are also being investigated. The most promising of these is extreme-ultraviolet lithography (EUV), which shrinks features using a very short wavelength of 13.5nm. Unfortunately, EUV requires a technological development that will not be ready for production before 2012. In the meanwhile, the best solution is to extend the use of immersion lithography through so-called ‘double patterning.’ At IMEC we are exploring this approach as a timely solution toward the 22nm half-pitch (hp) technology node.

The goal of double patterning is to improve resolution of dense circuit layouts by splitting them into two separate, sparser layers, imaging them separately, and recombining the images into the target pattern through the fabrication process. For example, an array of lines at 44nm pitch is made by recombining two arrays imaged separately, each at 88nm pitch. The essential components of the technique are, first, the physical process—i.e., the sequence of steps required to transfer a design layout into a patterned layer on a wafer—and, second, the decomposition of the design (splitting). In the double-patterning process, the initial image needs to be frozen to keep it from interacting with the second image in photoresist. Etching the first image into a sacrificial layer is one way of achieving this, but more cost-effective solutions are being developed.1

Figure 1. A coloring conflict in a 2D pattern is solved by cutting a polygon. At the cut position, stitching is ensured by locally overlapping the stitched polygons.

Figure 2. The stitching overlap partially reintroduces the dense pitch and small gap for imaging. The pitch, overlap, and gap dimensions are expressed in nanometers.

The design split of a 1D array of lines assigns every other design polygon to a different color or layer: an easy coloring problem. On the other hand, the design split of 2D layouts may lead to conflicts that—in the best case—can be solved by cutting existing polygons to increase the degree of freedom for coloring. The cut polygons must recombine through double patterning at ‘stitching points’ (see Figure 1). However, such points are potentially vulnerable to process variations. We have developed a method of studying the conditions for robust double patterning by identifying proper split and design guidelines.2 Here, the first

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metal-interconnect layer of random logic applications at 45 and 32nm hp, where double patterning is considered as a potential solution, is of particular interest. By systematically examining representative split test patterns, we have identified fundamental reasons for stitching failures and thus also the conditions under which the stitching is robust despite process variations.

Patterns from the two separate imaging steps need to overlap at the stitching points to compensate for line-end shape and position variations caused by dose, focus, mask, and overlay errors. As a result, subresolution pitch or gaps may be reintroduced (see Figure 2) where the goal was to double the pitch or remove the gap. At these locations, the imaging resolution limits the benefit of double patterning. For example, robust stitching of parallel split lines cut in the middle is only possible with a relaxed (i.e., larger) pitch (see Figure 3). Moreover, unrestricted designs, in particular random layouts for logic applications, highlight the difficulty of printing critical small gaps and pitch together. This is not compliant with double patterning, which requires relieving part of the pitch or gap constraints (see Figure 4) to improve resolution. Increasing the dimensions of the cut polygons also helps to ensure stitching robustness.

In summary, double patterning provides a means of extending the use of water-immersion lithography toward the 22nm node. Simply shrinking the unrestricted designs from previous nodes may result not only in split conflicts but also in failed stitching. For this reason, only a compliant design and well-tuned cutting and stitching will guarantee an acceptable yield (number of usable chips per wafer) when using double patterning at its highest resolution. The ultimate success of the technology depends on how adequate the designs are and whether more cost-effective patterning process flows can be developed. As next steps, we plan to work on optimizing the conditions for improving the patterning resolution of split layouts. We are also investigating the manufacturability of different freezing techniques.

Figure 3. Example of a random 45nm M1 (first metal-interconnect layer) logic test pattern after double patterning. Robust stitching through process variations requires increasing the pitch. (left) Split design. (right) Target image on the wafer.

Figure 4. Example of a regular 45nm M1 logic test pattern after double patterning. Relaxing the design in one direction allows robust double patterning at 90nm pitch. (left) Split design. (right) Target image on the wafer.

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References