Adhesion lithography for fabrication of printed radio-frequency diodes

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An innovative technique is used to pattern ultrahigh-aspect-ratio coplanar electrodes and to enable inexpensive, high-throughput printing of devices on large-area, flexible substrates.

Radio-frequency (RF) diodes are quintessential elements of passive RF identification tags that are used on livestock, luxury objects, and healthcare products. They are also used in near-field communication applications that enable wireless data transfer between devices. An RF diode—when matched to a suitable antenna—picks up the alternating current (AC) signal that is emitted from an RF source and transforms it to a DC signal. The DC signal can then be used to decode the information stored in the tagged object, or to simply power another electronic or optoelectronic device (e.g., a sensor, battery, or LED). The high demand for RF-harvesting devices, however, can only fully be met if their fabrication costs are substantially reduced. To realize this reduction in cost, novel printing technologies that permit manufacturing on large substrates are required. With these technologies it should be possible to ascertain that an increased diode performance (in terms of a small voltage drop, minimum leakage current, and a large gamut of operating frequencies) is attained.

At present, the most common approach for fabrication of printed RF diodes relies on the deposition of a high-mobility semiconducting material between two dissimilar (asymmetric) electrodes: see Figure 1(a). This architecture, however, suffers from numerous inherent drawbacks, including high resistor-capacitor time constants (which scale with device dimensions) and poor reliability (caused by pinholes that occur in the semiconducting layer when its thickness is less than 20nm). One way to circumvent these drawbacks is to use a coplanar diode architecture, as shown in Figure 1(b). Despite the numerous advantages of these coplanar nanogap electrode architectures, little effort has previously been devoted to their development. This is mainly because of the high cost and low throughput of patterning techniques that are currently available for their fabrication (e.g., electron beam or scanning probe lithography).

We have therefore developed an innovative patterning technique that is highly scalable and could be used to successfully address the challenge of cost reduction in RF diode manufacturing. Our technique—known as adhesion

Figure 1. Schematic illustration of (a) sandwich (vertical) and (b) coplanar (lateral) architectures for fabrication of metal–semiconductor–metal diodes. The active area of the diode is given by the width (W) multiplied by the length (L) of the electrodes, and d is the thickness of the semiconductor that separates the two metal (M1 and M2) electrodes.

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lithography (a-Lith)—is based on the modification of adhesion forces between two metal surfaces. We achieve this by functionalizing the patterned surface of one of the electrodes—i.e., M1 in Figure 1(b)—with a suitable self-assembled monolayer (SAM). This makes the surface hydrophobic and weakens its adhesion to the second metal layer—i.e., M2 in Figure 1(b)—that is deposited on top. By peeling off M2 with an adhesive tape, we can remove only the part of the metal that is in contact with the SAM, while the rest of the metal remains on the substrate. As a result, the two electrodes (which can be either the same or different material) are deposited next to each other and are separated only by the SAM molecules that isolate the electrodes and prevent their contact. Removal of the SAM thus results in an empty nanogap, which is typically less than 20nm: see the scanning electron microscope image in Figure 2(a). Finally, we deposit a high-carrier-mobility semiconductor within the nanogap structures to realize the fabrication of coplanar RF diodes.

In our technique, the process step that involves peeling off M2 is of the utmost importance for achieving consistent formation of uniform nanogaps. We have therefore developed a semi-automated system to perform controlled peeling of the adhesive tape. With the use of this system—see Figure 2(b)—the weakly bound part of M2 is removed from all the areas that overlap with M1, which thus creates the nanogap structure: see Figure 2(c). Our semi-automated system also allows us to assess the scalability potential of the a-Lith technique, as it can be applied on larger area substrates.

Once we optimized the production of our nanogap electrode structures, we were able to fabricate a number of coplanar RF nanodiodes (both on rigid glass and flexible plastic substrates). We based these nanodiodes on zinc oxide (ZnO) and buckminsterfullerene (C\textsubscript{60}) n-type semiconductors that are processed from solution at low temperatures. Such diodes exhibit high rectification ratios (RRs) and cut-off frequencies (exceeding the benchmark frequency of 13.56MHz, by far). More specifically, we attribute the exceptionally high performance (RR > 10\textsuperscript{6}) of our aluminum (Al)/ZnO/gold (Au) nanogap diodes to the excellent Schottky contact that is formed between the Au and ZnO.\textsuperscript{7}

We can further enhance the driving capabilities of our RF diodes by scaling the diode width. To do this, we devised interdigitated Al/Au nanogap structures—see Figure 3(a)—that are up to 1m in width. Despite the large electrode width, our coplanar nanogap diodes operate at low voltages (±2.5V) and are able to sustain a high forward current of 10mA (while the reverse current remains low, on the order of 10nA): see Figure 3(b). Furthermore, by optimizing the material deposition process (e.g., by increasing the number of ZnO layers from one to two), we achieve an increase in the DC output voltage (i.e., from 0.96 to 1.13V for an input AC voltage of ±3V at 13.56MHz): see Figure 3(c).

In summary, we have demonstrated our novel a-Lith patterning technique for the fabrication of high-performance n-type RF diodes. In the next steps of our work to further advance the a-Lith technique, we will demonstrate that we can use our...
approach to realize both p- and n-type diodes on arbitrary substrates (i.e., in terms of material and size). This will showcase that our technique has tremendous potential for process up-scaling. In addition, significant performance optimization and improved functionality can be achieved by making intelligent material selections and engineering choices. a-Lith is therefore a uniquely capable approach within the field of large-area electronics.

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**References**