A novel approach to semiconductor fabrication reduces both edge-placement error and the number of required block masks, and has application in device development for the 5nm node and beyond.

Since its first appearance in 1965, Moore’s law (i.e., the observation that the density of transistors on integrated circuits doubles approximately every two years) has survived many threats to its perpetuity. In fact, it has thrived for the past 20 years.\textsuperscript{1,2} With the semiconductor industry on the cusp of the N5 (5nm) technology node, however, this status quo is changing, and—as has been announced by many integrated-device manufacturers and foundries\textsuperscript{3,4}—areal scaling is approaching a slowdown. One of the key factors to overcoming this slowdown lies in obtaining control over the variability that creeps in during fabrication, leading to yield degradation.\textsuperscript{5} In patterning, this variability has been quantified as the edge-placement error (EPE). Simply defined, the EPE is the difference between the intended design and the actual on-silicon results. Controlling EPE at N5 and beyond is one of the foremost challenges for semiconductor fabrication.

In the development of advanced technology nodes, interconnects in integrated circuits represent a major area for which EPE control is a key factor.\textsuperscript{5} Critical back-end-of-the-line (BEOL) trench patterning at the N5 node requires a sub-30nm pitch line-space pattern. This small pitch (i.e., center-to-center distance between features) can be achieved using high volume manufacturing (HVM)-ready 193nm immersion-lithography-based self-aligned quadruple patterning (SAQP). However, block patterning (i.e., cutting an as-generated grid into a desired pattern) remains a challenge in terms of EPE. The standard approach for block patterning is shown in Figure\textsuperscript{1}. For both 193nm immersion-based and 13.5nm extreme UV (EUV)-based block patterning, multiple bright-field pillar-mask-based lithography passes are required (i.e., 4–5 and 2–3 masks, respectively). At the N5 node, this approach is challenging due to two major issues.

First, the aspect ratio of the pillar-block mask is too high, thus increasing the risk of flop-over. Second (and most critical), a pillar block placed on the wrong adjacent trench can cause an electrical open circuit. To avoid this outcome, the overlay requirement (i.e., the necessary alignment accuracy between the block and grid masks) is very strict (typically less than half-pitch). These

\begin{figure}[h]
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\caption{(a) Traditional block-mask approach for critical back-end-of-the-line trench patterning on a line grid defined by spacers (i.e., material A). Vertical gray and white lines show the eventual locations of dielectric material and metal wires, respectively (i.e., after metallization). The pink ellipse represents the block mask. Transparent ellipses show examples of bad overlay (with respect to the trench). In such cases, the block mask may cause electrical short circuits. (b) Our multicolor-material-based approach, in which each color designates a different etch selectivity. In our approach, every other trench is filled with a different sacrificial material (i.e., B and C, which would be a spin-on metal and a type of silicon, respectively). By introducing alternate materials in each trench, overlay variation is made trivial. Based on our calculations, this approach reduces the negative effects of overlay by three times compared to the approach shown in (a).}
\end{figure}
Figure 2. (a) Illustrations showing the step-by-step fabrication of our self-aligned block strategy for a standard self-aligned multiple-pattern (SAMP) integration scheme. Choice of the materials A, B, C, and D depends on relative etch selectivities. Typical examples are silicon dioxide, spin-on metal, silicon, and spin-on glass, respectively.

approaches are therefore challenging to implement in an HVM environment. Furthermore, because the overlay forms a large fraction of the overall EPE budget for circuit fabrication, the standard approach for block patterning is unfeasible for sub-30nm pitch trench patterning.

We have devised an alternate block-patterning approach that uses high etch selectivity between different patterning stack materials, thus achieving self-alignment for the block pattern with respect to the trench grid. Our method has the potential to significantly reduce the overlay requirement and the number of block masks that are required.

The details of our alternate block-patterning approach are shown in Figure 2. For our grid pattern, formed by self-aligned multiple patterning, odd and even trenches (mandrel side and spacer side, respectively) are filled with two types of sacrificial material. Self-alignment is achieved using a high etch selectivity while etching the trench material (with respect to the spacer material), thereby significantly improving the overlay. This results in a new overlay budget of three times half-pitch and hence improves the EPE. This approach enables us to use hole masks instead of pillar masks for selective etching of the trench material, after which a tone-reversal material (e.g., spin-on carbon, glass, or metal) can be employed to form the final block pattern. Our approach offers a significant advantage in pattern fidelity for both 193nm immersion-based and 13.5nm EUV-based approaches in terms of the flop-over margin. Further, by utilizing the selectivity between every alternate trench material, the original block can thus be decomposed into a potentially reduced number of masks.

The key underlying enabler for this alternate self-alignment-based block-patterning approach is etch selectivity. The etch selectivity represents a significantly more manageable approach than the traditionally implemented lithographic overlay method, which arises as a complex function of the integration, design, and prior-processing steps carried out on the wafer. As shown in Figure 2, high selectivity for etching the sacrificial materials (with respect to all other materials that are exposed during the patterning process) is crucial. Figure 3 shows an example of block patterning for the SAQP grid at 32nm pitch, and the selective-etching results. The multilayer stack (comprising a spacer, mandrel, and spin-on material)—see Figure 3(a)—is selectively cut into during the block-patterning process: see Figure 3(b) and (c). We will present further details of this work at the upcoming SPIE Advanced Lithography conference.6

In summary, we have introduced the concept of self-aligned block patterning for N5 and beyond. This approach has the potential to enhance the EPE (via overlay improvement) and to reduce the number of block masks that are required during fabrication. We have shown preliminary results for one example of its implementation for a 32nm-pitch grid, patterned via SAQP. In future work, we will focus on evaluating our concept...
Figure 3. X-ray secondary-emission microscope images showing the implementation of the self-aligned block approach on an SAQP-printed 32nm-pitch grid pattern with an oxide spacer, spin-on 3rd color material, and an inorganic mandrel (A, B, and C, respectively). ‘Color’ material denotes materials that have a high etch contrast with respect to one another. The selective removal of the material (b) B and (c) C is also shown.

with respect to real N5-standard cell designs to quantify the EPE improvement, and to benchmark different material libraries for its implementation.

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Nihar Mohanty is currently working in patterning integration development for N5 and beyond. He previously worked in etch development for dielectric etches in BEOL and middle-of-the-line (at N20 and N10), and patterning etches in front-end-of-the-line and BEOL (at N10 and N7).

References
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