Self-aligned quadruple patterning to meet requirements for fins with high density

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Repeated plasma deposition and etching steps enable the patterning of fins with the potential to meet requirements of N7 and N5 technologies for profile, depth, uniformity, and pitch walk.

Over recent decades, continuous reductions in the scale of field-effect transistors in accordance with Moore’s law, which states that the number of transistors in an integrated circuit doubles every two years, have enabled continuous increases in device performance and transistor density.1–3 Currently, state-of-the-art devices are based on structural elements with dimensions of 7nm or even 5nm (N7/N5). The highest-resolution patterns required for N7/N5 devices are silicon fins with a pitch of 18–28nm and metal layers with a pitch of 24–32nm. These dimensions far exceed the resolution attainable with 193 immersion (193i) lithography. Extreme UV lithography might be an alternative process for the formation of lines and spaces, but is expensive and not entirely ready for use in production.4

To overcome the limitations of lithography, multiple patterning methods—litho-etch or self-aligned multiple patterning—were used in the last four stages of device miniaturization based on nodes of 10–28nm (N10–N28).5,6 To achieve the specifications for fins in N7/N5 devices, we need a self-aligned quadruple patterning (SAQP) method that provides a critical dimension (CD) in the sub-nanometer range (3 sigma). As well as controlling the CDU, we developed plasma etching processes that generate vertical profiles, paying special attention to the mandrels. Figure 2 shows transmission electron microscopy (TEM) cross-sectional images of each SAQP step until the nitride pad etching step. After we completed the fin patterning, our preliminary results were as follows: a fin top CD of 7nm (measured by TEM); a fin CDU of 0.6nm (3 sigma); an average pitch walk of 0.5nm with a 3 sigma of 0.8nm; and a fin height of 115nm with a straighter profile on the top 50nm (see Figure 3).

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Figure 2. Transmission electron microscopy (TEM) images of the stages of SAQP show, from left to right: patterning of the first core onto a mandrel; deposition of SiO$_2$ by ALD; etching of the first spacers; etching of the mandrel to produce the second core; further deposition of SiO$_2$ by ALD; and etching of the second spacers and silicon nitride pad.

Figure 3. From left to right: top view of pattern obtained by critical dimension scanning electron microscopy (CDSEM) after SAQP, including etching and wet cleaning by hydrofluoric acid (HF); contour map and analysis of the pitch walk over a complete wafer based on CDSEM data; and TEM images of fins after etching and wet cleaning by HF. The sample preparation for TEM generates voids that distort the structure of the fins.

Figure 4. Left: Analysis of power spectral density (PSD) after lithography shows that the line edge roughness (LER) was lower than the line width roughness (LWR). Right: Analysis of PSD after SAQP shows that the LER was lower than the LWR in the high-frequency region and higher in the middle- and low-frequency regions.

In contrast to the sub-nanometer fin CDU and pitch walk, the exacting specifications for LER and LWR were more challenging to attain. After lithography, we carried out a roughness analysis of 131 images across a wafer of 300mm. The average values of LWR and LER were 4.2 and 2.9nm, respectively, which confirms that the line edges were uncorrelated (see Figure 4, left). After SAQP, a roughness analysis revealed that the LWR was about 1.2nm and the LER about 2.2nm, which suggests that the line edges were correlated. After etching of fins, analysis of power spectral density (PSD) showed that the LER was lower than the LWR at high frequency ($10^{-1}$ to $10^{-1.7}\text{nm}^{-1}$). However, the major contribution to the high LER is found at middle and low frequencies ($10^{-1.7}$ to $10^{-3.5}\text{nm}^{-1}$), which suggests that the lines became wavy at low frequencies.

Note that one of the most important factors in achieving high performance in SAQP is the reliance on measurement techniques, which need to have sufficient resolution to determine the roughness of small features. We have optimized the settings

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of CD scanning electron microscopy, such as averaging, field of view, and pixel size, for the determination of LER and LWR.\textsuperscript{7} We have also demonstrated the interpretation and feed-forward of data from scatterometry to improve the control of pitch walk.\textsuperscript{8}

The performance of SAQP that we have achieved is quite close to the specifications of the technology. However, the control of certain parameters needs to be improved, such as the control of LWR and LER at the photoresist level and during the etching steps. We have identified key methods that promise to enable improvements in LER (soft-plasma treatment of the photore sist), pitch walk (optimizing plasma-enhanced ALD), and CDU and profile (optimizing the etching process). Simulations using Coventor software will be used to test our assumptions in order to attain the target specifications.

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