Nanoimprint lithography and nanodefect management for semiconductor fabrication

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Nanoimprint technology combined with defect management could significantly reduce the cost of lithography for fabricating semiconductor devices.

Many industry experts believe that continuous shrinkage of semiconductor device design rules (DRs)—the parameters for checking lithographic mask correctness—is unsustainable. Nevertheless, DR shrinkage is still increasingly required for devices that use dynamic random-access memory (DRAM), negative- and (NAND) flash, 3D memory, resistive random-access memory (ReRAM), and systems-on-chip (SOCs) (see Figure 1). Furthermore, the arrival of big data will likely cause an information explosion that will prompt an exponential increase in demand for maximum memory capacity. 3D memory has very high potential to meet targets for both capacity and cost. However, at present its processing costs still exceed those of 2D memory. Therefore, the market requires a non-volatile semiconductor memory device that has improved reliability for data retention, and which will meet the rapidly increasing demand for storage.

The cost of implementing pattern-shrinking technologies, such as multi-patterning and extreme UV lithography (EUVL), is expected to grow substantially through 2019. Therefore, to significantly reduce lithography investment costs, researchers have been developing nanoimprint lithography (NIL). One of the most significant challenges in implementing this technology is achieving nanodefect management (NDM), which includes inspection of templates, imprinted wafers, and resist material for defects, and then undertaking appropriate mitigation. Enabling these processes has required intensive collaboration between providers of templates, nanoimprint lithography equipment, resists, metrology, and inspection and cleaning equipment. In addition, computational lithography technology enables prediction and correction of specific problems with nanoimprints. Furthermore, high-precision resist pattern etching at 20nm and below is critical for NIL and EUVL, and resist defects are generated after etching. Therefore, innovation in resist materials is required for all developing lithography technologies.

We used NIL technology to improve current devices, and we are now verifying the technologies and the compatibility of NIL to fabrication with silicon, in preparation for the production line. We need to solve the unique challenges of defectivity, overlay accuracy, and productivity. Specifically, we have to understand new phenomena in lithography, such as the influence of polymer rearrangement on liquid resist nanofluid mechanisms, and the effect of nanobubbles on metal ions in the material. Polymer rearrangement occurs at the wall of a channel, and causes the boundary layer between the wall and the resist to be stagnant. It also alters the viscosity of the resist close to the wall. Figure 2 shows the overlay accuracy on...


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the wafer edge according to the resist layer thickness, which also influences the resist viscosity. This in turn deforms the template, and the polymer rearrangement on the wafer. For overlay accuracy, we need to consider rearrangement of the polymer in the resist design. Moreover, this template innovation will lead to new NIL technology, enabling NIL to sub-20nm single patterning, which would improve template performance in terms of resolution, defectivity, critical dimension uniformity, and internal placement.

In summary, the intensive pursuit of large-scale integration downsizing to sub-2nm precision requires both pattern shrinking and cost reduction to enable manufacturing. Nanoscaled defects and particles are increasingly the main contributors to yield losses, and the developer’s greatest concern will be management of these. To address this challenge, we will in future use advanced metrology and inspection, such as electron beam (EB) inspection of wafers for multi-critical-dimension scanning electron microscopy. We will also need to adapt resists and materials, using, for example, etching resistance improvement and EB cure technology for templates. These processes will require super clean tools and clean-room environments to mitigate defects and/or particles for all unit processes.

Figure 2. Edge placement overlay accuracy depends on residual layer thickness. Si: Silicon. A1, A2, A3: Resist samples.

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References