Integrated light sources on silicon

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Heteroepitaxial lateral overgrowth of indium phosphide on silicon offers a pathway for monolithic integration of III–V light sources.

Over the last two decades, optical fibers and lasers have completely changed the way we communicate from vacuum tubes to integrated electronics. The data processing speed of an electronic chip has increased, but the data transfer speed between and within electronic chips still relies on slow copper-based interconnects. We need a system where data can be transported between chips in a faster and more efficient manner. One simple solution to this is to use light signals instead of electrical signals. There is an acute need for optical interconnects, which would increase data transmission speeds and efficiency, and reduce chips’ power consumption, area, size, and ecological footprint. However, although silicon, the basic electronic material that is used to produce electrical signals, is an excellent carrier of light signals, it cannot produce light signals.

In contrast, III–V materials—combinations of members of groups III and V of the periodic table—are excellent light sources. It is natural to think of integrating these two materials to tap the benefits of both, but their lattice constants (the spacing between atoms in the crystal lattice) are different. This results in highly defective material that is not suitable for device fabrication. Integration schemes based on bonding different materials have been proposed, but although these are viable and promising approaches to start with, in the long run, integrating the materials into one piece is desirable for low-cost, high-yield fabrication.

An attractive alternative to bonding approaches is epitaxial lateral overgrowth (ELOG): see Figure 1. ELOG, a fairly simple technique, exploits selective area growth (SAG) through openings in a thin film of dielectric material to annihilate threading defects generated at the polar (III–V) and non-polar (silicon) interface. By shrinking the SAG opening, we can reduce the probability of defect propagation to a very low level. Despite this, some defects are able to permeate through these openings. However, studies of these threading defects for specific material systems (in this case face-centered cubic) have revealed the exact directions and angles of these defects. We know that by orienting the openings at specific angles and maintaining an aspect ratio of 2 between the opening size and mask thickness, we can prevent the threading defects from being introduced into the ELOG layer.

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Earlier simulations from our lab showed that the dielectric mask used for defect filtering can be transformed into a silicon waveguide, buried in a silicon dioxide (SiO$_2$) cladding layer, to promote growth of a

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platform for evanescent coupling of the optical mode from the III–V stack with silicon. For efficient confinement of this light (optical mode) in the silicon waveguide, a fairly thick SiO$_2$ (2μm) cladding layer is required. However, such a thick mask makes it possible to enlarge the opening size and still maintain the required aspect ratio of 2, and these wide openings also permit the heat generated by the III–V light source to dissipate.

Based on these principles, we took a highly defective (4×10^9 cm$^{-2}$) indium phosphide (InP) seed layer predeposited on the (001) crystal surface of a silicon wafer and 4° off-oriented toward the <111> direction. The off-orientation is to prevent defects, known as antiphase domains or boundaries, where atoms in the crystal lattice are arranged in the order opposite to what is expected of a perfect lattice arrangement. These are usually formed when a polar material with diatomic steps (III–Vs) is grown on a material with monoatomic steps (silicon). Off-orientation introduces atomic steps in the substrate during wafer dicing. An even degree of off-orientation signifies the presence of diatomic steps on the wafer. We deposited a 2μm-thick layer of SiO$_2$ to mimic the earlier proposed buried SiO$_2$-Si-SiO$_2$ waveguide structure.

We used optical lithography to define multiple line openings with a width of 1μm and a length of 1.5cm, 20μm from each other to cover an overall area of 1.5×1.5cm$^2$. By optimizing reactive ion etching, we achieved smooth and vertical sidewalls using the photoresist as an etch mask. We optimized ELOG using hydride vapor phase epitaxy for isolated mesas (platforms) of InP on silicon, as ELOG layers generate new defects when they coalesce.

Continuing work on these ELOG InP on silicon layers, we grew multiple quantum wells (MQWs) based on indium gallium arsenide phosphide (InGaAsP) on top of the ELOG InP layer using metal organic vapor phase epitaxy. For light emission from the MQWs, clean and uniform interfaces between quantum wells and barriers are required, and transmission electron microscopy confirmed these (see Figure 2). The MQWs on the ELOG InP layer have shown comparable light emission intensity (>85%) with those on planar InP reference grown along with it, which supports the view that MQWs grown on isolated areas of InP on silicon are superior in quality. It also shows that ELOG has successfully integrated III–V materials on silicon without compromising the desired light emission.

In summary, we have demonstrated the promising nature of the ELOG technique, which can provide a true platform for monolithic integration of III–V materials on silicon. Through our proposed technology, light can be generated in a stack of epitaxially grown layers of III–Vs on silicon. This light can then be transferred to a waveguide made up of the same silicon, to communicate the light signal to the electronic chip. The beauty of this process is that it can provide epitaxially grown ultra-small light sources on silicon. We believe that we are close to our goal of achieving a monolithically integrated platform of III–Vs and silicon, which would solve the problem of slow copper-based electrical interconnects. We are now working to fabricate light sources for integration into circuits. Initial devices have shown optical resonances. These resonances support the high quality of III–V materials grown on silicon.

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Himanshu Kataria is a doctoral student at KTH. He has acted as a guest editor of Physica Status Solidi C. His research interests include heteroepitaxy of III–V materials on silicon for photonic integration and their photovoltaic application and processing.

Figure 2. Focused ion beam lamella removed perpendicular to the line openings. Inset: Transmission electron micrograph of indium gallium arsenide phosphide (InGaAsP) multiple quantum wells (MQWs) grown on top of the ELOG InP on Si.

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Sebastian Lourdudoss, currently a professor of semiconductor materials at KTH, has more than 28 years’ experience in semiconductor materials, devices, and processing. His expertise includes advanced epitaxial methods, nanofabrication, buried heterostructure lasers, photonic integration, and heteroepitaxial solutions for III–V materials on silicon.

References