A mixed design approach yields a high-performance processor able to meet the requirements of future space missions.

In recent years the complexity of space-oriented applications has grown dramatically. The data rates and volumes produced by both scientific and commercial space missions have increased significantly, thus creating an urgent need for better data-processing technologies. Onboard analysis of sensing data before transmission to Earth is becoming vital for satellites and spacecraft to effectively exploit bandwidth to ground stations. The currently available space-qualified European digital signal processor (DSP) is no longer adequate to the task, and US-made products are strongly regulated and increase dependence on critical technology from outside Europe.

Since 2007, the European Space Agency (ESA) has emphasized the need for a new generation of high-performance, general-purpose space-qualified DSPs, spurring a number of initiatives in the field. Although radiation hardening of commercial products provides a fast, temporary fix, a long-term solution to computational demand will require DSP architectures specifically designed to be radiation-hardened. Our objective in the European project DSPACE (DSP for Space Applications) is to develop a new DSP architecture for space applications that provides significantly enhanced performance compared with the previous generation of processors, along with a software development environment (SDE).

Starting from a LISA (Language for Instruction Set Architectures) model of the DSPACE processing unit, we concurrently generated a ‘synthesizable’ hardware description, written in VHDL (VHSIC Hardware Description Language), and the related software tools (assembler, linker, and simulator). We developed the rest of the building blocks (caches, memory and bus controllers, interfaces, and so forth) following a traditional hardware design flow based on hand-written VHDL (i.e., code produced by a digital designer as opposed to being automatically generated from the high-level LISA model of the processor). The reuse of an open-source GCC (GNU Compiler Collection)-based tool chain avoided the cost of developing a C compiler. A specific software layer translates and optimizes GCC into DSPACE assembly code, which is then passed through the LISA-generated software tools. As a result, the final code is optimized for the specific DSPACE processing architecture.

Figure 1 shows a schematic diagram of the high-level DSPACE system-on-chip (SoC) block. To achieve a significant increase in performance over previous DSPs without relying on high clock frequency, the core leverages a pipelined and massively parallel architecture based on the VLIW (very long instruction

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word) paradigm: sixty-four 32-bit registers, four arithmetic logic units, four multipliers, and two address-generation units. The SoC runs up to eight RISC (reduced instruction set computing) instructions per cycle, processing 32-bit fixed or IEEE single-precision floating-point operands. The rest of the DSPACE architecture consists of a 32KB instruction cache and 64KB data cache with error detection and correction (EDAC), direct memory access for communicating with the off-chip main memory, a DDR (double data rate) memory controller, and two SpaceWire interfaces for high-speed transfer between the SoC and the hosting system (e.g., to read the status of a sensor). Finally, AMBA (advanced microcontroller bus architecture) buses connect the building elements.

To validate the performance of the system, using the benchmarks established in 2008 by ESA, we designed a demonstrator board based on a Xilinx field-programmable gate array (see Figure 2). The entire SoC occupies 30% of the resource budget on this device, operating at a clock frequency of 60MHz. The printed circuit board of the demonstrator is about the size of a 3U compact computer bus interconnect and includes a DDR2 SODIMM (small outline dual in-line memory module) connector with 2GB of onboard memory and various space interfaces: i.e., SpaceWire, CAN (controller area network), and MIL1553. The board can be housed in a CompactPCI crate or alternatively in a stand-alone box.

Toward the future realization of a space-qualified ASIC (application-specific integrated circuit), a preliminary implementation of the DSP SoC on a CMOS standard 180nm cell library shows an area of around 380k gates, and a peak performance of 1GOPS (giga operations per second) and 750MFLOPS (mega floating-point operations per second) at 125MHz. The Atmel ATC18RHA is the target European space technology. But to increase the speed and reduce the power consumption of the ASIC, we will also consider the ST DSM65 65nm technology. First results on FIR (finite-impulse-response) filtering benchmark, evaluated for different filter lengths (ranging from 16 to 1024 bits) and various output lengths (ranging from 128 to 1024 bits), show a performance similar to fast ground DSPs such as the TMSC67xx by Texas Instruments and, in terms of computational power/clock frequency, the Analog Devices ADSP-21469.

In summary, the DSPACE DSP implements ESA requirements for the next generation of space DSPs to meet increasing demand for onboard processing in future missions. The aggregated peak performance of 1GOPS (750MFLOPS) at 125MHz outperforms the currently available European space-qualified DSP by 17 and 13 times, respectively. The high-performance cache-aided architecture and its wide instruction set make it possible to handle the large variety of space applications (e.g., lossless data compression, image processing, and data fusion). In the coming months the demonstration board will be realized and made available to the space community, as will the final results of the synthesis—i.e., the automatic translation of the VHDL design description to the logic—and the benchmark tests.

The research leading to these results has received funding from the European Community’s Seventh Framework Programme (FP7/2007–2013) under grant 262798. We would like to thank the software architects of Space Application (Belgium), RWTH Aachen University (Germany), and Intecs SpA (Italy) for contributing the SDE and their support in tuning the architecture.

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