Large-scale photonic integration: a key-enabling technology for all-optical signal processing

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The first multi-format-processing-chip, comprising more than 50 passive and active elements, enables format-independent wavelength conversion and regeneration of data signals at different bit rates.

Emerging services and applications—such as 3D TV, video on demand, and peer-to-peer applications—are driving network capacity and cost to their limit. Current research and standardization efforts are focusing on the use of advanced modulation formats such as differential-phase-shift keying (DPSK) and differential-quadrature-phase-shift keying (DQPSK) to increase optical-fiber bandwidth capacity. For the foreseeable future, these advanced modulation formats will have to co-exist with standard on-off keying (OOK) due to already-installed fiber-transmission equipment.

In this context, photonic integration is a key enabling technology toward the aggregation of complex functionalities for multiple modulation formats on single photonic chips. One such initiative is supported by the European Commission through the ICT-APACHE project.\(^1\) It aims to develop multi-format transmitters, receivers, and regenerators based on hybrid integration of high-performance indium phosphide (InP) monolithic elements on low-loss planar silica-on-silicon circuits. Hybrid integration has numerous advantages, such as low loss and power consumption, and a small footprint. However, the most significant benefit is easy adaptation of the silica motherboard to different circuit designs and a wide range of applications. Here, we describe a multi-format-processing chip (MFPC) that we fabricated for the first demonstration of multi-format regeneration and wavelength conversion on a single device.\(^2\) Until now, this capability has only been possible using discrete devices interconnected with bulk fibers.\(^3\)

Figure 1(a) presents the MFPC layout, comprising four semiconductor optical amplifiers (SOAs) in two nested Mach-Zehnder interferometric (MZI) structures, two pairs of delay interferometers (DIs) with 22 and 44 GHz free spectral range (FSR), 15 thermo-optic phase shifters (labeled A–O), 31 passive optical couplers, and 32 input and output pigtailed ports. Figure 2(b) Continued on next page
Figure 2. Concept of operation for (a) OOK, (b) DPSK, and (c) DQPSK data signals. DPSK: Differential-phase-shift keying. DQPSK: Differential-quadrature-phase-shift keying. λ1, 2: Wavelength. OOK: On-off keying.

shows the MFPC mask design, and Figure 2(c) illustrates the silica motherboard with dimensions 38 × 87mm². The MFPC is capable of supporting OOK operation at variable input bit rates and DPSK/DQPSK operation at 22 and 44Gbaud. Dual-channel operation, using combinations of OOK and DPSK data signals at different wavelengths, is also feasible on a single chip.

Regeneration of OOK signals is based on the standard operation of the SOA-MZI nonlinear gate by means of cross-gain modulation and cross-phase modulation occurring in the SOAs between the input data signal at λ1 and the clock signal at λ2: see Figure 2(a). In the case of DPSK signals—see Figure 2(b)—a DI with FSR that equals the input bit rate is used in front of the SOA-MZI for decoding the phase information into amplitude. The two complementary decoded OOK streams serve as control signals into the SOA-MZI that is now operated in differential mode and yields the PSK output at the converted wavelength λ2. In the case of DQPSK signals, a pair of DIs followed by parallel SOA-MZI structures in a nested configuration yields the two PSK signals at λ2 with a differential phase shift of π/2rad that reconstruct the wavelength-converted QPSK output.4

We have evaluated the regenerative performance of the MFPC for degraded OOK and DPSK input signals. For this, we have introduced amplified spontaneous emission (ASE) noise and phase noise to the input signals, and we have compared their bit-error ratio (BER) before and after the multi-format regenerator at 22Gbaud. Figure 3(a) depicts the results for the OOK input signal that is degraded due to ASE noise by a power penalty of 3.5dB at BER 10⁻⁹ with respect to reference back-to-back measurements. We have measured 1.5dB performance improvement of the regenerated output with respect to the degraded input. ASE-noise suppression is performed by the nonlinear SOA-MZI gate, which that acts as an optical power limiter under saturation. This reduces the amplitude fluctuations around the mean power of the marks and is also illustrated in the eye diagrams in the inset of Figure 3(a).5

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Figure 3(b) shows the performance of the MFPC for an ASE-loaded DPSK signal degraded by 3dB at BER $10^{-9}$. It shows 1.1dB improvement for the decoded output PSK stream with respect to the decoded degraded input. ASE-noise suppression relies on the same mechanism as for the OOK format, although fluctuations in the amplitude of the decoded streams may induce small phase noise to the output PSK signal after the SOA-MZI. This is negligible in our case, due to the small $\alpha$-factor (~3–4) of the nonlinear SOAs. Figure 3(c) shows the results for DPSK regeneration when the input signal is loaded with phase noise corresponding to initial degradation 2dB at BER $10^{-9}$. We observed 1.4dB performance improvement, verifying that phase noise is the favorable type of signal distortion. Efficient phase-noise suppression is attributed to the nonlinear transfer function of the DI around the ideal ‘1’ and ‘−1’ DPSK states.

With their large scale and complex functionality, photonic integrated chips are a key step on the roadmap to system development that will sustain the exponential growth of traffic in next-generation transparent optical networks. Besides enhancing performance and being cost-effective, they promise an energy-prudent approach for the telecoms industry. In this article, in a proof by example, we have shown that format-independent, all-optical signal processing can be realized with the hybrid integration of InP monolithic chips on silica-on-silicon substrates. We anticipate that more and more complex functionalities will be accommodated on the same chip in the very near future. Our next step will be to exploit our hybrid integration technology by designing and developing integrated transmitter and receiver arrays with polarization-multiplexing potential.

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