Heterogeneous transmission and parallel computing platform for remote sensing

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A novel architecture promises a new approach to real-time data post-processing for advanced satellite-navigation systems.

Global navigation satellite system reflectometry (GNSS-R) is a remote-sensing technique that receives and processes microwave signals that are reflected from various surfaces. The system is shown schematically in Figure 1(a). The global positioning system open-loop differential real-time receiver (GOLD-RTR) instrument has been proposed as a complement to GNSS-R to gather global positioning system (GPS) satellite signals after they have been reflected from surfaces such as sea, ice, and ground\(^1\) and to extract useful information from them: see Figure 1(b). This configuration—called the GNSS-R scenario—was first proposed in 1993 by the European Space Agency (ESA) as a passive multistatic radar system for monitoring mesoscale ocean altimetry. The main and most innovative feature of GOLD-RTR is its computation and storage in real time of the complex-valued cross-correlation waveform (CC-WAV) between GPS L1-C/A (so-called legacy civilian navigation) signals and the reflection signals. The CC-WAV retrieves geophysical parameters over different types of surfaces, e.g., sea level and tides, ice roughness and thickness, and soil moisture and biomass.

However, the growing number of satellite installations is making great demands on high-performance post-processing design for space-level instrumentation. Due to the intensive computation required for CC-WAV and the amount of data that must be stored prior to downlinking, onboard real-time parallel processing has been suggested as a promising approach to GNSS-R post-processing systems. Previously,\(^2\) we proposed reducing the link load between satellite and ground by integrating the CC-WAV for one second by incoherently adding (i.e., averaging) the different points of the surface from the reflected waveform and comparing the result with the corresponding direct signal. Here, we describe a method of post-processing the CC-WAV on a space segment to lessen the data transmission load on the ground.

In the past 10 years, dynamically reconfigurable field-programmable gate arrays (FPGAs) have proven well suited to parallel architectures because they incorporate several soft cores (i.e., open cores and embedded operating systems). Taking into account time-to-market issues and rapid prototype development, a shared-memory symmetric multiprocessor (SMP) mounted with an embedded operating system would appear

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to be the obvious choice. However, bus-based SMPs have limited scalability due to bus congestion and shared memory issues. The advent of network-on-a-chip (NOC) separates computation and communication architectures. Compared with symmetric multiprocessing, NOC enhances system throughput and scalability. By the same token, it is not easily adapted to the ever-changing protocols and memory allocation of network processors. Our novel on-board parallel processing architecture—heterogeneous transmission and parallel computing platform (HTPCP)—separates the transmission and the parallel processing loads into two modules to meet the timing required by the application: see Figure 1(d).

The HTPCP consists of a GR-CPCI-XC4V LEON Compact PCI (PCI Industrial Computers Manufacturers Group) development board plus its extension board GR-CPCI-2ETH-SRAM-8M. This combination serves as the interface between the GOLD-RTR and the control PC: see Figure 1(c). We introduce a single-correlation integration (SCI) algorithm to lessen the storage requirement of the CC-WAV by processing it in real time.

As shown in Figure 2, real-time geophysical parameters are transmitted from the GOLD-RTR to the HTPCP through an Ethernet interface, and distributed to eight processing units (PUs) by two transmission units (TUs) in the HTPCP. Each PU processes the consecutive one-millisecond waveforms of one channel in parallel. Meanwhile, each TU accomplishes two tasks: data storage and data distribution. Each unit has its own memory and bus, which are accessible from the local processor. The memory hierarchy of TUs and PUs is distinct. The individual memory size varies with bandwidth. The software framework can accommodate different stacking approaches. The interconnections between TUs and PUs are effected by means of a fast simplex link, which consists of a nonlatency register-to-memory single-direction communication path. The interconnections between TUs are established by a message-passing interface (MPI) to realize the interactions between the GOLD-RTR and the control PC. The MPI is capable of receiving commands from one remote processor and passing them to another remote processor.

transparently, and synchronizing packet transmission with local traffic.

We present the evaluation methodology followed by a comparison of timing performance in an SMP architectures versus the proposed HTPCP. To analyze the cache-memory gap and the memory-bus gap in SMP, we implement a series of simulations based on the MPARM and uClinux simulator. The simulation results are intended to illustrate the improvement in execution time and the system throughput of the HTPCP. Numerical results of our analyses show that system throughput can reach up to 1.669MB/s. SCI processing time is 8.17 times faster compared with conventional coarse-grained parallelism in symmetric multiprocessing applications.

In summary, the HTPCP offers a means of balancing the uneven workload of transmission and processing. Although our prototype employs the SCI algorithm, it could in future be used with other CC-WAV algorithms. We have also shown that the real-time hardware performance of the HTPCP exceeds that of symmetric multiprocessor. As a next step, we plan to apply our instrument in a real-world example to validate our proposed method.

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References