Ultimate low-power devices

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Self-powered, integrated systems-on-a-chip are key to developing extremely low-power devices for applications in commercial, defense, space, harsh-environment, and medical settings.

In today’s world, consumer-driven technology is eyeing self-powered, handheld electronic gadgets. We are, therefore, working on reducing power consumption and supplying sufficient power to run such integrated devices. Ever-increasing consumer demand for more powerful mobile devices is driving the search for longer-lasting energy sources. In addition, harsh-environment applications, such as those used in the oil and gas industries, deep-sea exploration, and remote sensing, require long-lasting, unmanned devices.

To achieve this energy independence at the nanoscale, several critical technical challenges must be overcome, including nanofabrication of macro/microsystems. This requires developments incorporating light weight (thus portability), low power consumption, faster response, higher sensitivity, and batch production (low cost). In addition, advanced nanomaterials must be integrated to meet performance/cost targets. Nanomaterials may offer new functionalities that were previously underused at macro/microscale dimensions. Finally, energy efficiency must be achieved to reduce power consumption but still supply enough power to meet that low-power demand.

With these challenges in mind, we focus on the concept of an energy-independent system-on-a-chip (SoC) (see Figure 1). Our proposed device includes power-consuming and power-generating parts. The former consists of the main control unit, the communications circuit, and sensors. Collectively, they are responsible for controlling power supply to the load application. The power-generation section consists of a rechargeable lithium-ion battery, a microbial fuel cell, a thermoelectric generator, a solar cell, and a piezo-electric energy harvester. DC power is drawn from the battery, while the microbial fuel cell and thermoelectric generator serve as on-chip battery chargers.

We have worked extensively on high-k (dielectric constant)/metal-gate-stack-based, low-standby-power devices for the 45nm technology node and beyond using both planar and non-planar architectures.1–3 Our results show significant leakage-current reduction in the off state while attaining higher drive current for faster computation (see Figure 2). Since classical charge-transport-based devices will always fall short of beating the subthreshold slope of 60mV/decade, we also demonstrated electromechanical switching (physical attachment and isolation-based relay) at sub-100nm scales (see Figure 3).4,5

Figure 1. Self-powered, integrated systems-on-a-chip. LIB: Lithium-ion battery. PNG: Piezo-electric energy harvester. TEG: Thermoelectric generator. uMFC: Microbial fuel cell.

Figure 2. A high $I_{on}/I_{off}$ current ratio ($5 \times 10^5$) is achieved without any strain engineering (engr.) at a positive supply voltage, $V_{dd} = 1V$. Continued on next page...
This type of device and its hybrid integration (combined with charge-transport-based devices) may enable fabrication of circuitry where high-performance computation is achieved using charge-transport devices and low-power operations are carried out by nano-electromechanical switches. We are also developing advanced nanofabrication technology for controlled integration of 1D nanowires and nanotubes that are compatible with the state-of-the-art CMOS-based platform. With intelligent circuit design and integration of smart, low-power transistors, we expect to develop ultralow to no-power-consumption circuit components.

While we continue to reduce power consumption on the SoC’s ‘debit’ side, we are focusing on integrating energy-scavenging and storage devices, materials, and components. As we experience increased power dissipation and, thus, heated back surfaces of laptops, we show that (by integrating thin-film thermoelectric generators) we can take advantage of the thermal difference of the hot surface (up to 65°C) and room temperature (around 25°C), and convert it into electricity to run approximately 45,000 transistors on a 45nm-node chip. This effort represents our group’s core objective to turn negative effects (recyclability) into positive opportunities. We are also working on improving the design of microbial fuel cells for integration with the SoC. Our recent design shows that we can introduce much higher surface-to-volume ratios than any previous demonstrations (see Figure 4).

In summary, we propose that energy-independent SoCs may operate in harsh-environment conditions characterized by significant temperature differences, changes in pressure, or abundant solar energy. SoCs may or may not be subjected to all these conditions at the same time. The idea is to harvest energy from whatever condition is available at any given time and place. We estimate that the maximum power that can be generated with the energy-independent SoC and high-\(k\)/metal gates, with all power-generation components active, is between 5.51 and 9.5mW. The recently developed Phoenix processor is a very-low-power device that consumes only 39pW. We estimate that an even larger number of transistors can be employed with carbon-nanotube and nanowire technology.

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Muhammad Hussain obtained his PhD in electrical engineering from the University of Texas at Austin in December 2005. He is currently an assistant professor in electrical engineering, and has authored 71 peer-reviewed international journal and conference papers on nanofabrication. He is also editor-in-chief of the *Journal of Applied Nanoscience* (Springer).

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References


