Accurate top-down processing of silicon photonic devices

Zhiping Zhou

Combining electron-beam lithography, inductively coupled plasma etching, and atomic-layer-deposition techniques achieves carefully controlled fabrication of nanophotonic devices.

As nanotechnological developments reach the realm of practical applications, the demand for accurate nanofabrication techniques increases. The latter involve accurate control of device sizes, shapes, and locations. For example, integrating nanophotonic devices into silicon microelectronic chips requires device reduction to micrometer scales, with a sidewall roughness in the nanometer range, to minimize optical losses. In addition, for chip-scale integration of photonic crystals (PCs), accurate control of their critical dimensions and exact locations is extremely important to achieve predetermined performance goals. To meet these challenges, we have developed a number of top-down processing approaches by incorporating electron-beam lithography (EBL), inductively coupled plasma (ICP) etching, and atomic-layer-deposition (ALD) techniques to obtain well-controlled and cleanly located features.

Our techniques involve fabricating a silicon microring resonator with smooth sidewalls. Sidewall roughness is normally induced by the transfer of both mask-edge and etched-surface roughness. The latter results from chemical reactions and ion bombardment on the silicon sidewall during etching, which may be controlled by selecting proper processing gases.) We investigated the transfer of mask-edge roughness very carefully using EBL and ICP etching based on three different mask materials deposited on top of silicon-on-insulator wafers, including chromium (Cr) and negative electron-beam resist (specifically, MaN-2403 and hydrogen silsesquioxane: HSQ).

We patterned the Cr mask through a lift-off process, but to completely remove all Cr around the waveguide patterns was very difficult because of molecular forces. This results in severe edge roughness (see Figure 1), which is subsequently transferred to the etched-silicon sidewall during ICP etching. The final roughness is approximately 40nm, resulting from the combined roughness of the Cr mask and ICP etching (see Figure 2).

Figure 1. Roughness at the edge of the chromium (Cr) mask.

Figure 2. Silicon-sidewall roughness.

The mask-edge roughness of both MaN-2403 and HSQ is relatively small, usually several nanometers, and determined by the resist properties. Obtaining the MaN-2403 and HSQ masks is simpler because it does not involve lift-off. Since the silicon-etch selectivity to HSQ is much higher than to MaN-2403 for chlorine (Cl₂) plasma, thinner HSQ masks are needed to etch the same amount of silicon. The thinner mask will further improve the

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Table 1. Comparison of fabrication processes.

<table>
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<tr>
<th>Process</th>
<th>Sidewall complexity</th>
<th>Process latitude</th>
<th>Sidewall roughness</th>
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<tbody>
<tr>
<td>Cr mask</td>
<td>complicated</td>
<td>excellent</td>
<td>rough</td>
</tr>
<tr>
<td>MaN-2403 mask</td>
<td>simple</td>
<td>poor</td>
<td>smooth</td>
</tr>
<tr>
<td>HSQ mask</td>
<td>simple</td>
<td>good</td>
<td>smooth</td>
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Figure 3. Fabrication of silicon microring resonators using different masking processes: (a) Cr, (b) MaN-2403, and (c) HSQ-mask etching.

EBL resolution and reduce the mask-edge roughness. Cl₂ and perfluorocyclobutane (C₄F₈) are used for silicon ICP etching of the MaN-2403 and Cr masks. This takes advantage of polymer protection from C₄F₈ for the etched-silicon sidewalls. For silicon etching with the HSQ mask, we only apply Cl₂, since C₄F₈ corrupts HSQ, the silicon oxide-based polymer.

We compared process complexity and latitude, as well as sidewall roughness in Table 1 (see Figure 3). This demonstrates that using HSQ masks, optimized ICP etching, and without any post-etch process, the sidewall roughness of silicon waveguides is less than 10nm,¹ which is 2–3 times better than previously reported.

We developed a second processing technique for photonic crystal (PC) fabrication by atomic-layer deposition (ALD) with sacrificial etching.² In many applications, PC devices are needed with a full band gap for all polarizations. Therefore, we propose a novel type of 2D, polarization-insensitive PCs, ‘annular photonic crystals’ (APCs):³ see Figure 4. These are composed of dielectric rods and circular air holes in a triangular lattice such that the rods are centered in the holes. This is the most difficult aspect of the fabrication process: since the air gap is generally less than 50nm, very precise alignment is required for positioning the dielectric rods.

We established a self-alignment procedure using ALD and sacrificial etching. Since the alignment precision of this two-step process is determined by ALD, it can be controlled to within 1–2Å, i.e., the thickness of one atomic layer. A carefully controlled etching using a combination of diluted and standard buffered oxide etch (a mixture of hydrofluoric acid and ammonium fluoride), results in the final APC structure (see Figure 5). This demonstrates, for the first time, a fabrication protocol to form an APC structure that may be used for polarization-insensitive applications. Avoiding the challenging EBL alignment, this novel method can achieve alignment accuracy down to the atomic level.

In conclusion, we demonstrated two top-down processing approaches for nanophotonic-device fabrication on a silicon platform. By combining EBL, ICP etching, and ALD, we achieved less than 10nm sidewall smoothness and atomic-level alignment accuracy without the need for other post-etch processes. Our next step will be to fabricate novel, functional photonic devices on a silicon platform using these methods.

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Figure 5. Final annular photonic-crystal structure accomplished by a combination of diluted and normal buffered oxide etch, which optimizes the undercut effect of wet etching.

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References