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San Jose Marriott and San Jose Convention Center
San Jose, California, USA

Conferences & Courses
26 February–2 March 2017

Exhibition
28 February–1 March 2017
Present and publish your work at the world’s premier semiconductor lithography event.

Call for Papers

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DATES

Conferences & Courses: 26 February–2 March 2017
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LOCATION
San Jose Marriott and San Jose Convention Center
San Jose, California, USA

DATES

2017
For over 40 years, the SPIE Advanced Lithography Symposium has played a key role in bringing together the microlithography communities involved with semiconductor devices, micro-/nano-systems, and related fields. Advances in traditional patterning together with the growth of alternative approaches drive the solutions of these demanding technologies. In the semiconductor field, the challenges of manufacturable, cost-effective lithography continue as patterning is extended further toward physical limits. State-of-the-art processes are being advanced through immersion lithography combined with multiple patterning and design co-optimization. Extreme UV lithography continues to move closer to volume production readiness, with a long string of successes along the way. And the lithography community is aggressively pursuing new patterning approaches to drive the implementation of complementary solutions. Success calls for unique interdisciplinary interactions and coordinated efforts between lithographers, layout designers, materials scientists, and metrology/process control engineers to enable cost efficient patterning solutions.

A full spectrum of lithography and patterning topics are encompassed by this year’s symposium across seven complementary conferences. Participants come from a broad array of backgrounds to share and learn about state-of-the-art lithographic tools, resists, metrology, materials, etch, design, and process integration. Through a series of provocative panel discussions and seminars, the symposium also probes current issues being faced as we extend current methods, move toward alternative approaches, and identify new ways to complement one technology with another. SPIE Advanced Lithography Symposium also provides the unique and primary forum for meeting and interacting with a wide range of industry experts, researchers, and key players working on patterning technology development. Attendance ensures that participants learn and share the latest developments in areas of central importance to many vital technology fields.

This year, the SPIE Advanced Lithography Symposium is structured into the following conferences. All conferences are organized by current practitioners of the art working together with organizing committees of experts in these fields. Joint sessions between the conferences also offer opportunities to cover topics common across these interest areas.

- Emerging Patterning Technologies
- Extreme Ultraviolet Lithography
- Metrology, Inspection, and Process Control for Microlithography
- Advances in Patterning Materials and Processing Technology
- Optical Microlithography
- Design-Process-Technology Co-optimization for Manufacturability
- Advanced Etch Technology for Nanopatterning

We welcome your participation for the 2017 SPIE Advanced Lithography Symposium and urge you to submit your abstracts to the appropriate conference as described in the Call for Papers, and be sure to tell your colleagues to do the same. Relevant topics for new technology groups, keynote talks, or panel discussions are also solicited.

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Rochester Institute of Technology

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Extreme Ultraviolet (EUV) Lithography VIII (AL101)

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In 2016 among the many EUVL tools now deployed, dramatic increases in EUV source power and throughput were achieved. In 2017, chip-makers will be focused on driving EUVL technology toward meeting HVM productivity and yield targets for the 7-nm logic technology node. Nevertheless, a number of critical technology challenges remain. For example: meeting productivity and availability targets for HVM; improving mask yield, inspection, review, and repair infrastructure, and weighing pellicle options; simultaneously improving resist resolution, sensitivity and LER. Looking beyond the 7-nm node, progress will require innovative approaches in EUV sources, for both higher power and coherence control strategies, continued development of mask architecture and imaging materials, and consensus on the creation of imaging systems and masks for higher numerical apertures or magnifications. Despite decades of work, new advances in all EUV research areas demonstrate that improvements are always possible, toward the moving target of commercialization and timing.

The Extreme Ultraviolet Lithography conference continues to be the leading forum for scientists and engineers from around the world to present and discuss research on the advancement of EUV lithography technologies. This conference welcomes submissions of original papers that emphasize recent advances in the many areas related to EUV lithography technologies, and efforts toward commercialization.

Technical and scientific papers advancing the state of the art in EUV Lithography in the following areas are solicited:

**PATTERNING**
- integration learning and OPC
- in fab inspection and control
- double-patterning EUVL
- imaging simulations and source-mask optimization
- cost of ownership
- yield

**MASKS**
- substrates and blanks
- aerial imaging and patterned mask inspection
- absorber patterning
- mask roughness
- reticle handling solutions
- pellicle development and platform integration
- coatings for higher numerical apertures
- flare-reduction technologies

**EXPOSURE TOOLS**
- imaging performance
- focus, dose, and overlay control
- aberrations, flare, and out-of-band light
- optics design and fabrication
- multilayer coatings
- high-NA or anamorphic imaging systems

**SOURCES**
- power scaling
- efficiency and reliability
- source characterization
- source collectors, cleaning, and lifetime
- new concepts

**EUV RESISTS**
- resolution
- line-edge roughness
- sensitivity improvement
- out-of-band sensitivity
- etch transfer
- emerging materials and novel chemistries

**LIFETIME**
- environment control
- surface contamination and cleaning
- capping layers
- particle contamination, mitigation and removal
- resist outgassing
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Emerging Patterning Technologies 2017 (AL102)

Conference Chair:
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Our conference showcases emerging lithography and patterning techniques that provide solutions for scaling semiconductor IC nodes (i.e., 7 nm technology IC nodes and beyond), wafer level packaging, and non-IC related technologies such as MEMS, Display, Photonics, Roll-to-Roll, Meta-materials, Micro-Fluidics, 3D printing, additive manufacturing. Contributions are also welcome which create hybrid approaches which employ a combination of lithographic aerial imaging and patterning processes such as self-aligned pitch division, tone-reversals, selective depositions, directed self-assembly, etc.

APPLICATION AREAS FOR EMERGING PATTERNING TECHNOLOGIES
• semiconductor 7nm IC nodes and beyond
• semiconductor wafer level packaging and fan-out
• bioelectronics and genomics
• photovoltaics and related energy applications
• disk drives and patterned media
• large area display/flat panel displays
• roll to roll/web format device manufacturing
• bioelectronics and LEDs
• photonic crystals and Meta-materials
• negative-refractive-index
• nanopatterned sensors, waveguides, antenna
• building blocks for defect tolerant computing
• smart resists and self-healing materials.

TECHNOLOGY AREAS FOR EMERGING PATTERNING TECHNOLOGIES:
DIRECT WRITE OR MASKLESS LITHOGRAPHY AND PATTERNING TECHNOLOGIES
• electron or ion charged particle beams
• optical beams
• STED (2-color) direct write
• resistless e-beam or ion beam direct patterning
• beam directed nucleation, ion beam deposition
• metal or ceramic powder sintering
• material ablation or material transformation reactions
• ink-jet
• scanning array lithography, dip-pen printing, etc.
• interference lithography, plasmonic or nearfield/evanescent wave
• micromirror optical lithography
• 3D metal or ceramic sintering.

PROCESS BASED LITHOGRAPHY AND PATTERNING
• directed self-assembly
• nanoimprint lithography
• selective deposition
• self-aligned or pitch division process integration techniques.

In the spirit of facilitating exchange of knowledge, we strongly encourage contributions in which information critical to understanding the topic is discussed.
Metrology, Inspection, and Process Control for Microlithography XXXI (AL103)

Conference Chair: 
Martha I. Sanchez, IBM Research - Almaden (USA)

Conference Co-Chair: 
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Metrology-based analysis, identification, and control of error sources continue to enable rapid evolution of optical microlithography. Metrology of exposure dose and focus supports ever smaller process windows. Dimensional metrology in layouts facilitates resolution enhancement and validation of control. Extremely tight overlay is required for multiple patterning. Development of materials, equipment, and processing in EUV, direct write, nanoimprint, directed self-assembly, and deposition drive further innovation of metrology tools and applications. This conference is the leading forum for the exchange of foundational information and discussion of novel concepts in patterning-related metrology and inspection. Consistent with the conference charter and goals, please submit original technical papers in these and related technology areas:

METROLOGY AND INSPECTION
- optical full-field and scanned microscopy, scatterometry and interference microscopy
- novel measurement techniques with high-resolution optics, scatterometry, SEM, AFM
- particle-beam scanned microscopy, materials characterization and elemental analysis
- design rules, design compliance, hot spots, design-based metrology and inspection
- metrology for design rules and process margins, budgeting, and budget control
- metrology for lithography development, patterning models build and validation
- metrology on photomasks, including pre-compensation, OPC, and phase shifting
- parametric electrical testing and other device performance-based metrology
- applications in emerging patterning technologies including optical immersion and EUV lithography, direct-write, nano-imprint, and directed self-assembly
- applications in manufacturing of ICs, cell stacking, wafer bonding, TSV and 3D integration, displays, thin-film heads, MEMS, MOEMS, bio-arrays, lab on the chip, integrated optoelectronics and other micro- and nano-systems.

CRITICAL DIMENSION, IMAGE PLACEMENT, AND OVERLAY
- 1D, 2D, and 3D metrology of CD and pattern placement, including within device layouts
- alignment, registration and overlay metrology, processing and metrology integration
- edge profile and edge placement, roughness of edge, width, and centerline
- optical, SEM, and AFM based in-die overlay on small targets and devices.

MEASUREMENT SYSTEM MODELING AND SIMULATION
- physics and mathematical models of metrology process and detection methods
- physical characterization of both systems and samples, model parameters
- data analysis methods, library-based image analysis, and algorithms.

CALIBRATION AND ACCURACY
- metrology quality, error diagnostics, and data culling
- measurement resolution and error, including precision and accuracy
- standards and reference materials, calibration methods, hybrid metrologies
- reference measurement systems and metrology comparisons
- tool fleet performance, maintenance, and matching.
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PROCESS CHARACTERIZATION, CONTROL, PERFORMANCE, AND YIELD

• process metrology and monitors, segmentation and reduction of variance
• metrology sampling, excursion detection, costs, device performance, and yield
• data analysis and visualization, process control, feedback and feed forward.

DEFECT DETECTION, ANALYSIS, AND CONTROL

• detection and control of pattern defects and across-wafer process variation
• environmental contamination, including impacts on processing and defects
• defect reduction, yield improvement, effective data use.

PERFORMANCE LIMITS IN METROLOGY AND INSPECTION

• responses to commanded skews and cross-technology comparisons
• models of tool-sample interaction, noise, and error mechanisms.

THE KAREL URBANEK MEMORIAL BEST STUDENT PAPER AWARD

This conference features the Karel Urbanek Best Student Paper Award sponsored by KLA-Tencor Corp. This award consists of an SPIE citation and an honorarium. The award recognizes the most promising contribution to the field by a student, based on the technical merit and persuasiveness of the paper presentation at the conference. To be eligible, the leading author and presenter of the paper must be a student.

To establish eligibility, the principal author’s bio submitted with the abstract must state the academic status and the institution, as well as the advisor’s name and contact information.

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Advances in Patterning Materials and Processes

Conference Chair:
Christoph K. Hohle, Fraunhofer Institute for Photonic Microsystems (Germany)

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Advances in patterning materials and processes are at the heart of innovation in the semiconductor industry. The development of high-performance resists and the continuous evolution of their applications and processing have been critical enablers for lithography technology improvements for all device generations. The limits of optical lithography have been extended, in no small part, by innovative materials and processes that expand and improve on fundamental resist progress to provide high-resolution, robust, and cost-effective technologies for both mass production and development of future device generations. Evolutionary and ultimately revolutionary innovations will be required in patterning processes and resist materials to achieve the combination of resolution, edge roughness, and sensitivity required for future technology nodes at the needed technological pace.

The Advances in Patterning Materials and Processes Conference continues to be the leading forum for scientists and engineers from institutes, material vendors, and end-users around the world to present and discuss research on the chemistry, physics, and performance of resist materials. Its scope encompasses the latest advances in patterning materials technology including patterning stack and process innovation, pitch division processes, template processing for self-assembling materials (DSA), imprint lithography (NIL), non-traditional scaling approaches (3D integration, etc.) and other topics.

This conference welcomes submissions of original papers that emphasize recent advances in high-performance patterning processes and materials and their integration in established, maturing, emerging, and new lithographic technologies.

Original technical papers are solicited, but not limited to the following traditional topics:

**MATERIALS AND PROCESSES FOR**
- EUV lithography
- 193nm (immersion) lithography
- longer UV wavelengths
- electron-beam lithography
- nanoimprint lithography (NIL)
- directed self-assembly (DSA)
- positive and negative tone materials and processes (PTD, NTD).

**PATTERNING FILMS AND APPLICATIONS**
- topcoats: contamination and reflection control
- underlayers: reflection control, pattern transfer, process enhancement
- multilayer integration
- chemistry and materials science of self-assembling materials (DSA)
- new pattern transfer approaches
- surface passivation
- selective deposition as an enabler for patterning.

**RESIST APPLICATIONS**
- single and multiple patterning
- implant processing
- templating for self-assembly
- chemically amplified and not amplified resists (CARs, non-CARs)
- materials for photonic applications, NEMS, MEMS and MOEMS
- thick films for SOC/SIP integration.
PROCESSING AND PROCESS CONTROL
• resist smoothing, rectification, trim and shrink
• tone inversion materials
• applied processing, including defect control and pattern collapse mitigation
• materials challenges related to etch, process control and metrology
• new processing techniques and applications, especially self-aligned strategies.

SIMULATION AND MODELING
• resist fundamentals
• materials chemistry and processing
• assessment of patterning and materials scaling limits
• variability, stochastics, and pattern formation
• design for or simulation of new processes and applications.

Abstracts, that are addressing overlapping topics with adjacent conferences of the SPIE Advanced Lithography symposium (e.g. EUV, DSA, Etch) may be arranged in appropriate joint sessions.

Consistent with the conference’s charter and goals, authors are required to provide a description of chemical and physical principles as well as sufficient chemical structural detail in presented work. Papers which do not reveal sufficient chemical details so as to add value to the readers or are principally of a commercial nature may not be accepted for presentation and publication.

IMPORTANT DATES
Abstracts Due:
6 SEPTEMBER 2016
Author Notification:
24 OCTOBER 2016
Manuscripts Due:
30 JANUARY 2017

Please Note: Submissions imply the intention of at least one author to pay registration, attend the meeting, make their presentation as scheduled whether it is a poster or an oral, and submit a 6-page (minimum) manuscript for publication in the conference Proceedings of SPIE in the SPIE Digital Library.
OPTICAL MICROLITHOGRAPHY

Conference Chair:
Andreas Erdmann, Fraunhofer-Institut für Integrerte Systeme und Bauelementetechnologie IISB
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Many innovations, the integration of new technologies and the continuous improvement of manufacturing techniques for lithographic equipment have enabled optical projection lithography to stay the primary lithographic technology for semiconductor manufacturing for about 40 years. After the introduction of high-NA ArF immersion technology, the progress of optical lithography is mainly related to the holistic optimization of lithographic systems and processes, and to an improved image and process control. In addition to resolution, edge placement error (EPE) control and high quality photomasks are required to support the application of material-driven resolution enhancements including double or multiple exposure/patterning and directed self-assembly (DSA). The successful use of optics to provide viable working solutions for future technology nodes will require fundamental integration of all aspects of the patterning process. Optical projection lithography will keep its dominating role in semiconductor manufacturing. However, cost-effective solutions and appropriate combinations with other lithographic techniques, including DSA, extreme ultraviolet lithography (EUV) and multiple-e-beam direct-write (MEBW) have to be identified to support the further scaling of semiconductor products.

Optical lithography is also used in many other areas of micro- and nanofabrication, including power semiconductors, silicon photonics, flat panel displays, MEMS, NEMS, microfluidics and biosensors. Although the required feature size is significantly larger than for high-end IC-fabrication, these applications come with other requirements such as special profile shapes, non-Manhatten layouts, extreme overlay and CD-uniformity requirements, extremely high topography, unbalanced pattern densities etc. Many of these applications use alternative optical exposure techniques ranging from mask proximity printing, gray tone techniques, interference lithography and Talbot imaging to innovative laser direct write techniques such as multi-wavelength and STED-inspired lithography for 3D patterning.

This conference welcomes abstract submissions covering topics that are advancing the field of optical nano- and microlithography for IC-fabrication and other areas of micro- and nanofabrication. Submissions on alternative exposure techniques and non-IC applications will be considered for joint sessions on “Advanced Lithography and Patterning for Emerging Markets”. Additional joint sessions of the SPIE Advanced Lithography symposium will address overlapping topics between optical lithography and design for manufacturing, materials and metrology.

Specific topics of this conference include, but not limited to:

**PUSHING THE LIMITS OF OPTICAL LITHOGRAPHY**
- optical lithography at kl < 0.3 options
- multiple exposure and multiple masking techniques including requirements and challenges of cut-masks
- novel illumination and mask types
- novel materials and processes to break optical diffraction limit
- alternative imaging methods: STED-inspired techniques, multi-color lithography, negative index and plasmonic lenses
- layout regularization and optimization to extend the limits of optical lithography
- design compliance towards multiple patterning/ SADP/SAQP
- complementary lithography with DSA, e-beam, EUV, imprint to extend resolution for optical lithography

**LITHOGRAPHIC IMAGING FUNDAMENTALS AND PROCESS INTEGRATION**
- multiple masking in manufacturing: results and issues
- process integration of resolution enhancement methods, CD shrink and multiple patterning techniques
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- Image and process analysis and assessment: Characterization and minimization of CD and overlay variation; EPE requirements in the context of multiple patterning
- Simulation of full systems and process components including rigorous modeling of optical, resist and mask effects
- Mask effects on imaging, including mask-induced focus shifts and aberrations
- Negative-tone processes and related modeling techniques
- LER reduction and analysis.

Computational Lithography
- Predictive modeling and verification
- Fast 3D mask and wafer topography models
- 3D resist and etch modeling for OPC
- Advanced pattern correction, OPC and verification
- Advanced pattern matching for hotspot detection
- Source mask pupil optimization (SMO) and inverse lithography technology (ILT)
- Advanced mask decomposition algorithms
- Model-based retargeting and layout modification to compensate process effects.

Lithography Tools and Subsystems
- Exposure tools and tracks that support multiple exposure processes
- Overlay control down to 2nm and below, including effects of grid matching
- Overlay mark optimization towards product feature placement
- Tool control for OPC stability and matching
- Through multiple layers integrated OPC and tool control
- Design and materials issues for imaging
- Advances in system design and integration
- Novel advances in system self-metrology
- Exposure tool and source developments
- Illumination metrology and control, including polarization
- Evaluation and characterization of lens performance
- Metrology systems for set-up, adjustment, and control
- Environmental health systems and contamination control.

Lithography Costs
- High-throughput tools and processes
- Productivity and cycle time improvement, advanced process control (APC)
- Process simplifications including “freezing” alternatives
- Product layout and cost considerations.

Optical Lithography for Non-IC Applications
- Silicon photonics and communications
- Flat panel and display applications
- MEMS, NEMS, and microfluidics
- Biological applications: biosensors and 3D skeletons for stimulation of cell growth
- Optical micro- and nanostructure fabrication
- Data storage applications such as HDD and patterned media
- Flexible electronics and organic electronics
- Lighting, PV and solar cells nanopatterning
- Micro-stereolithography
- Holographic applications
- Plasmonic applications
- Alternative exposure techniques.

Student Award

Students submitting papers to this conference only, will be considered for the Cymer Scientific Leadership Award for Best Student Paper. This award is given each year at this conference and recognizes extraordinary work achieved by students interested in the microlithography field, and strongly supports the contributions made to scientific advancement at the conference. The award includes a plaque along with a monetary award to help support the student’s future research activities.

All candidates for the Cymer award, including those who are placed as an oral presentation, are asked to present their work on a poster during the poster session for the Optical Microlithography conference.

If you are/have a student author or co-author that is making the presentation in the Optical Microlithography conference, please send your tracking number to Will Conley at: will_conley@cymer.com
Design-Process-Technology Co-optimization for Manufacturability XI (AL106)

Process-driven constraints to design have been a reality for multiple generations of semiconductor manufacturing, and design for manufacturability has become a widely adopted spectrum of tools and methods. This conference, aimed at technical and management professionals engaged with the interface between integrated circuit design and manufacturing, invites articles that examine novel approaches for design and process integration aimed at "more Moore" enablement, fast turn-around, cost-effectiveness, and high-yielding integrated circuit (IC) creation.

Contributions should emphasize fundamentals of technical solutions rather than their commercial embodiments. Submissions in design-for-manufacturability, circuit and yield characterization, and other interdisciplinary studies, including but not limited to those based on electronic design automation (EDA), are welcome.

Topics of interest include, but are not limited to:

**DESIGN FOR MANUFACTURING**
- physical layout optimization for advanced or novel patterning methodologies
- design and verification methodologies using novel manufacturing models
- layout optimization for systematic and random yield loss reduction
- layout optimization for minimizing circuit variability
- manufacturing friendly circuit design styles and methodologies
- DFM for "more than Moore" applications (analog, RF, digital/SoC, etc.).

**DESIGN-AWARE MANUFACTURING**
- leveraging design-intent information (beyond layout) for RET/OPC application
- propagating electrical design intent for RET/OPC optimization and verification
- performance-power-manufacturability (speed-leakage-RET) optimization.

**DESIGN AND MANUFACTURING CO-OPTIMIZATION**
- design for multipatterning (MP) technology
- design for directed self-assembly (DSA) technology
- design for interferometric lithography and novel subtractive and additive patterning techniques
- design-rule development strategies and methodologies
- layout style and lithography co-optimization (including optical source and design co-optimization)
- design-to-process simulation and calibration
- design-to-manufacturing methodologies for analog circuits, MEMs, and other microlithography applications.

**DESIGN-TO-MANUFACTURING ECONOMICS**
- cost-performance tradeoffs between design and manufacturing
- design to manufacturing flow methodologies for productivity improvement, time-to-market, and cost reduction
- new models for maximizing net return on investment in design and manufacturing.

Special consideration will be given to papers that emphasize methodologies for using manufacturing information in the design flow. Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.
Advanced Etch Technology for Nanopatterning VI (AL107)

Conference Chair: Sebastian U. Engemann, IBM Thomas J. Watson Research Ctr. (USA)

Conference Co-Chair: Rich Wise, Lam Research Corp. (USA)

Program Committee: Efrain Altmirano-Sánchez, IMEC (Belgium); Julie Bannister, Tokyo Electron America, Inc. (USA); Sang-Hoon Cho, SK Hynix, Inc. (Korea, Republic of); Maximse Darnon, LTM CNRS (France); Eric A. Hudson, Lam Research Corp. (USA); Catherine B. Labelle, GLOBALFOUNDRIES Inc. (USA); Nae-Eung Lee, Sungkyunkwan Univ. (Korea, Republic of); Qinghuang Lin, IBM Thomas J. Watson Research Ctr. (USA); Gottlieb S. Oehrlein, Univ. of Maryland, College Park (USA); Erwine Pargon, CNRS/LTM (France); Nicolas Posseme, CEA-LETI (France); Ricardo Ruiz, HGST (USA); Seiji Samukawa, Tohoku Univ. (Japan); Robert Turkot, Intel Corp. (USA); Jeff Xu, Qualcomm Technologies Inc. (USA); Anthony Yen, TSMC Taiwan (Taiwan); Ying Zhang, Applied Materials, Inc. (USA)

The revolution in microelectronics over the last 50 years of Moore’s law has been led by exponential increases in dimensional scaling of logic and memory semiconductor devices. Dramatic innovations in optical lithography have been the driving force behind much of the success of dimensional scaling. Challenges to direct wavelength and numerical aperture scaling have increasingly driven innovations in plasma based pattern transfer to extend scaling beyond the physical limits as defined by the Rayleigh criterion.

This new paradigm in scaling is the patterning era, utilizing innovative plasma processing techniques to dramatically extend the achievable pattern dimension and fidelity. It capitalizes on implementing etch and deposition processes into an overall patterning strategy to create new opportunities in “complementary patterning” for the basic elements common to all patterns (lines, spaces, holes). This new paradigm has redefined the role of next-generation lithography, etch, deposition and process control for scaling of semiconductor devices.

The increasing interdependence of lithography technologies, photoresist technologies, and plasma etch technologies has created new opportunities in materials, integration, and the co-optimization of plasma based patterning with lithography and process control. Looking beyond, semiconductor process and manufacturing knowledge in nanopatterning is now enabling new areas such as IoT and cognitive computing.

Original and overview technical papers are solicited on the following topics, but not limited to:

- novel developments in plasma based patterning techniques: EUV-based patterning, self-aligned spacer techniques (SAXP and mandrel/spacer design), DSA, nanoimprint, optical lithography patterning, complementary patterning, self-aligned structures, on product overlay.
- novel discoveries of plasma—material interactions: plasma-photoresist interactions, LER/LWR evolution, EUV resist interactions, MOL/BEOL (low-k) material interactions, novel substrate material handling (SiGe, III-V, C) etc.
- defect reduction or yield enhancement techniques by dry or wet process solutions.
- new etch methodologies and their application to patterning processes: atomic layer etching (ALE), low Te processing, etc.
- patterning control through advanced process solutions: in-situ process control, process simulations, etch aware OPC, edge place error (EPE) etc.
- novel patterning solutions for logic and memory applications.
- patterning solutions for emerging product applications (cognitive computing, quantum computing, IoT, etc.)

Special consideration will be given to papers that emphasize issues which are cross-disciplinary in nature.

Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.

IMPORTANT DATES

Abstracts Due: 6 SEPTEMBER 2016
Author Notification: 24 OCTOBER 2016
Manuscripts Due: 30 JANUARY 2017

Please Note: Submissions imply the intention of at least one author to pay registration, attend the meeting, make their presentation as scheduled whether it is a poster or an oral, and submit a 6-page (minimum) manuscript for publication in the conference Proceedings of SPIE in the SPIE Digital Library.

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Awards presented at the 2016 Metrology, Inspection, and Process Control for Microlithography Conference

The 2015 Diana Nyyssonen Memorial Award for Best Paper was presented to Narender Rana, Yunlin Zhang, Donald Wall, Bachir Dirahoui, Todd C. Bradley, IBM Semiconductor Research and Development Ctr. (USA) for their presentation Machine learning and predictive data analytics enabling metrology and process control in IC fabrication [9824-54]

The 2016 Karel Urbanek Best Student Paper Award was presented to Student, Maria Laura Gödecke, Univ. Stuttgart (Germany), and co-authors Sandy Peterhänsel, Karsten Frenner, Wolfgang Osten, Univ. Stuttgart (Germany) for their presentation Measurement of asymmetric side wall angles by coherent scanning Fourier scatterometry [9778-16]

Awards presented at the 2016 Advances in Patterning Materials and Processing Technology Conference

The 2015 C. Grant Willson Award for Best Paper was presented to Andrew Grenville, Jeremy T. Anderson, Benjamin L. Clark, Peter De Schepper, Joseph Edson, Michael Greer, Kai Jiang, Michael Kocsis, Stephen T. Meyers, Jason K. Stowers, Alan J. Telecky, Inpria Corp. (USA); Danilo De Simone, Geert Vandenberghe, IMEC (Belgium) for their presentation Integrated fab process for metal oxide EUV photoresist [9425-29]

The 2015 Hiroshi Ito Memorial Award for the Best Student Paper was presented to Arjun Singh, Boon Teik Chan, Roel Gronheid, IMEC (Belgium); Doni Parnell, Toyko Electron Ltd. (Netherlands); Hengpeng Wu, Jian Yin, Yi Cao, EMD Performance Materials Corp. (USA) for their presentation Patterning sub-25nm half-pitch hexagonal arrays of contact holes with chemo-epitaxial DSA guided by ArFi pre-patterns [9425-34]

The 2016 Jeffrey Byers Memorial Best Poster Award in Resist was presented to Kensuke Matsuzawa, Ryan A. Mesch, Wade Wang, C. Grant Willson, The Univ. of Texas at Austin (USA); Mike Olah, Scott Phillips, The Pennsylvania State Univ. (USA) for their presentation Aromatizing unzipping polyester for EUV photoresist [9425-64]

The 2016 Best Student Award in Microlithography was presented to Andrew Brubine, Bruce W. Smith, Rochester Institute of Technology (USA); John Sturtevant, David Fryer, Mentor Graphics Corp. (USA) for their presentation Bayesian inference for OPC modeling [9780-17]

The 2016 Best Student Award in Microlithography Conference

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The Fritz Zernike Award for Microlithography

The Fritz Zernike Award for Microlithography is given annually for outstanding accomplishments in microlithographic technology, especially those furthering the development of semiconductor lithographic imaging solutions. Yan Borodovsky, Intel Senior Fellow (Retired), was presented the 2016 Zernike Award in recognition of his efforts toward the advancement of multi-generational lithography process solutions and as a key contributor of patterning approaches and layout design rules at Intel.

The Special Contribution Award to the Art and Science of Lithography

The Special Contribution Award to the Art and Science of Lithography for outstanding contribution, visionary guidance, and inspiring dedication to the lithography community and to the SPIE Advanced Lithography symposium, was individually presented to William H. Arnold, ASML US, Inc. (USA) and Harry J. Levinson, GLOBALFOUNDRIES Inc. (USA).

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EXHIBITION: 28 FEBRUARY–1 MARCH 2017

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TECHNICAL PROGRAM
Available November 2016
The comprehensive Advance Technical Program will list conferences, paper titles, and authors in order of presentation. This piece provides an outline of all planned special events and hotel and registration information.

REGISTRATION
All participants, including invited speakers, contributed speakers, session chairs, co-chairs, and committee members must pay a registration fee. Fee information for conferences, courses, a registration form, and technical and general information will be available on the SPIE website in November 2016.

HOTELS
Opening of the hotel reservation process for Advanced Lithography is scheduled for November 2016. SPIE will arrange special discounted hotel rates for attendees that will be available when housing opens. Please do not call SPIE for information. The SPIE website will be kept current with any updates.

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Find important requirements for visiting the United States on the SPIE Advanced Lithography website. There are new steps that ALL visitors to the United States need to follow. Online at: spie.org/visa

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SPIE would like to express its deepest appreciation to the symposium chairs, conference chairs, program committees, session chairs, and authors who have so generously given their time and advice to make this symposium possible.

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